Waiting for the Post-CMOS Godot

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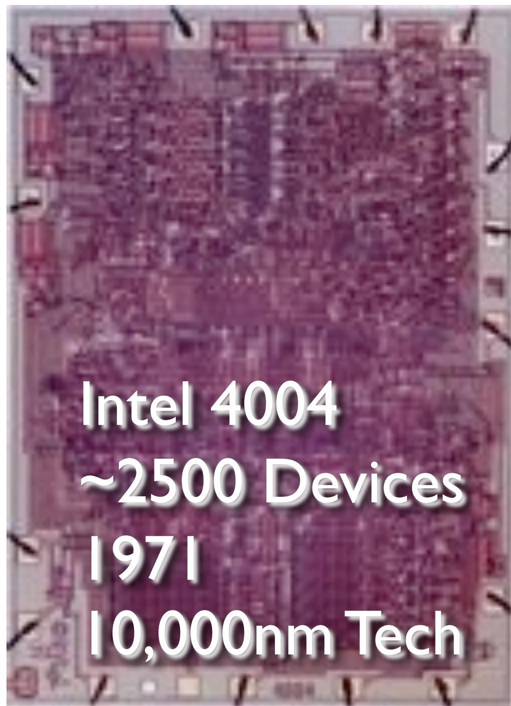
Introduction to the Play

- **Waiting for Godot** (/ˈɡɒdoʊ/ GOD-oh) is an absurdist play by Samuel Beckett, in which two characters, Vladimir and Estragon, wait endlessly and in vain for someone named Godot to arrive. Godot's absence, as well as numerous other aspects of the play, have led to many different interpretations since the play's premiere. It was voted "the most significant English language play of the 20th century”.

Source: Wikipedia.

A Brief Retrospective



1971 … 2011

10,000nm … 22nm

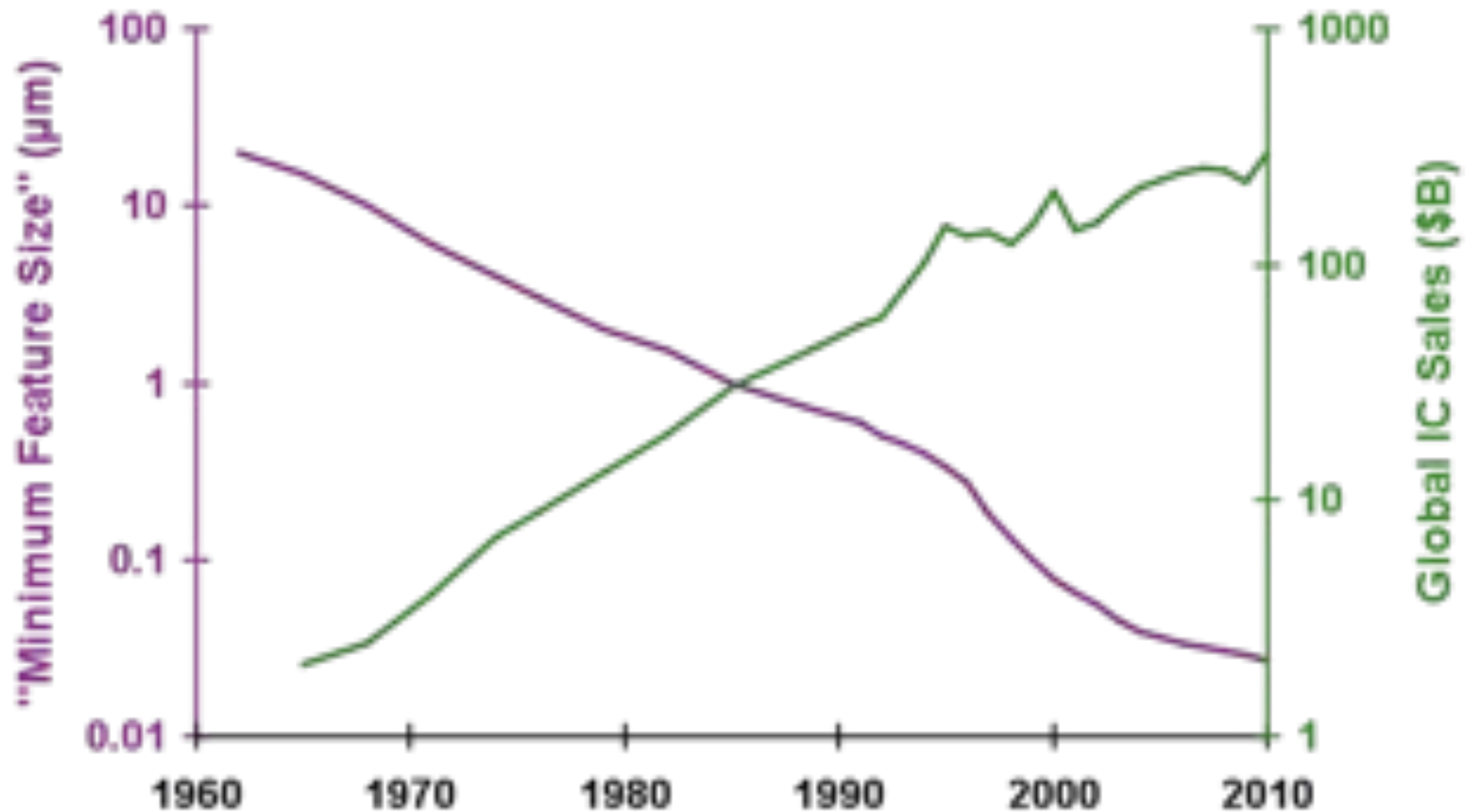
2^9 (~500) reduction in feature size

2^{18} (~65,000) increase in density

~18 process generations

And Still Going…

The Global Economic Impact...



What was the result?

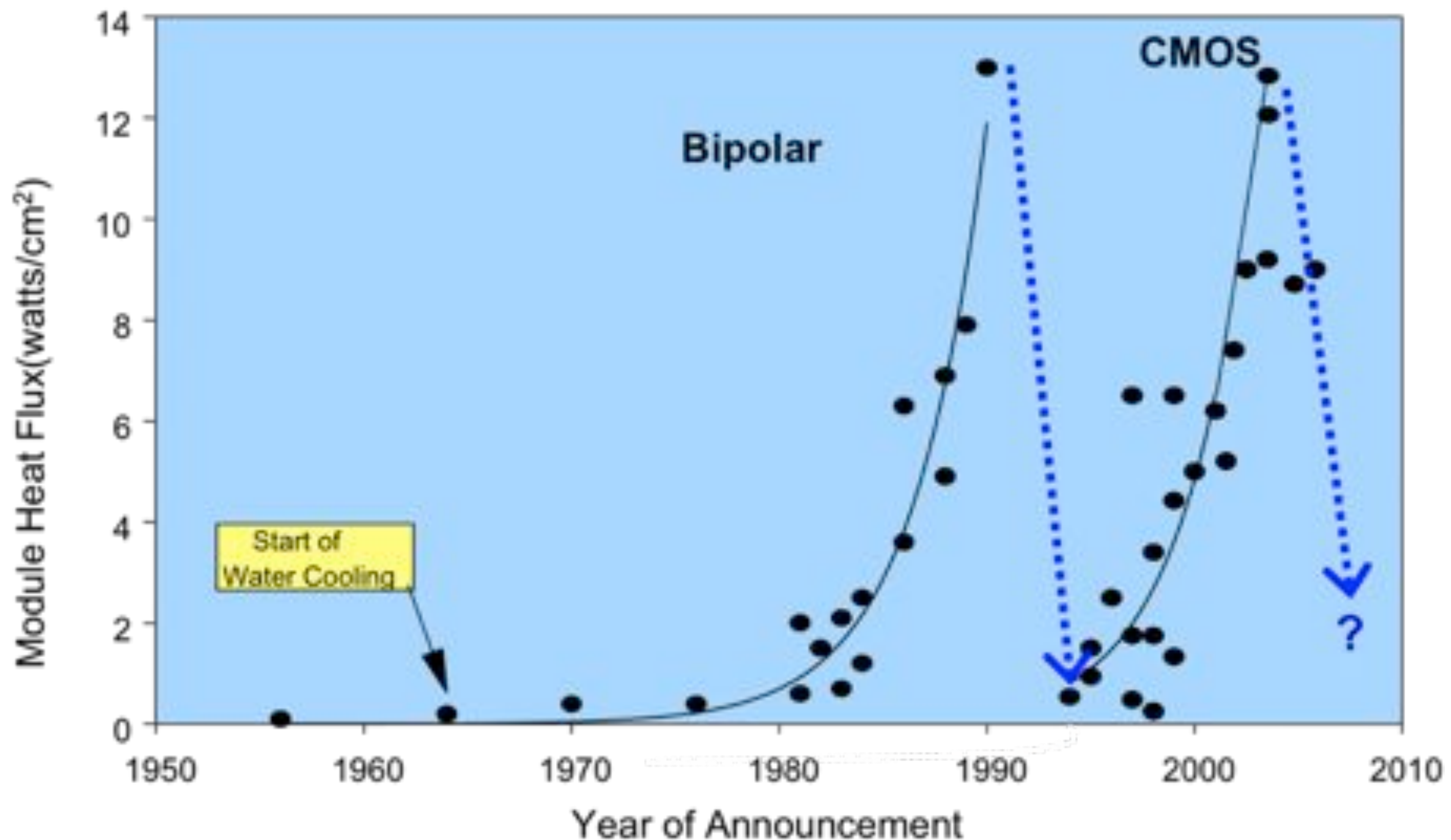
- The world relies on electrical engineers to build all the various devices on which our life runs.
  - Your phone and computer.
  - Your microwave and ATM.
  - Your brakes and your heart implant.

	1990	2007
Percent of households with:		
Television	98%	98%
Average number of sets per home	2.0	2.6
Share with Wired Cable Television	56%	62%
Share with Video Cassette Recorders	69%	90%
DVD Player	–	82%
Computer	22%	74%
Internet Access at Home	–	68%
Broadband	–	51%
Cellular Phone	5%	73%

- We have created an expectation that these devices just “work”.

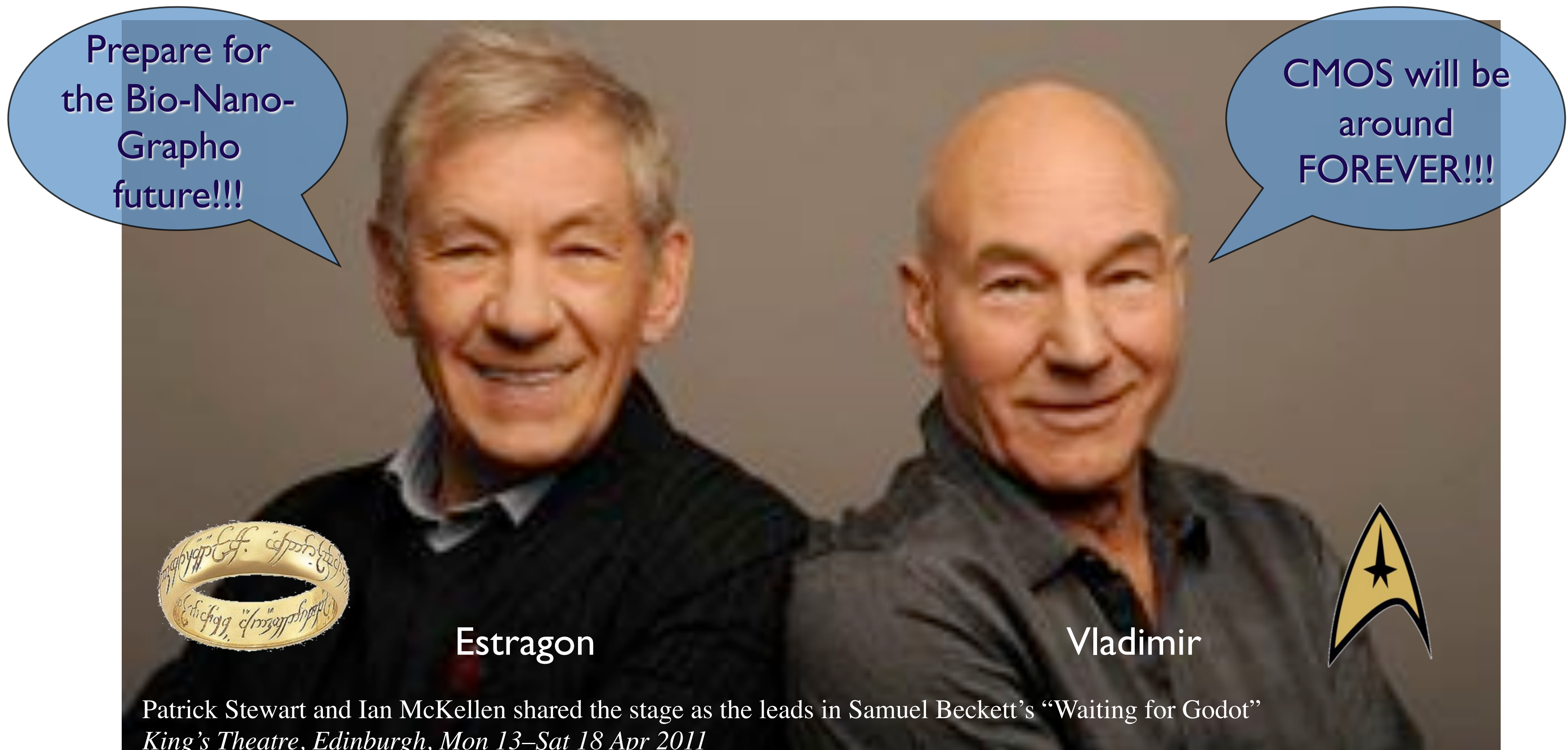
But... What does the future hold?

- Many were certain we could not break the 1000nm barrier.
  - The phrase “sub-micron challenges” was quite common.
- More recently... Power has been a major driver:



The Post-CMOS Dialogue

- What post? (there is no technology post CMOS).
- Post What? (the new technology will be so good we will not even think about CMOS any longer).

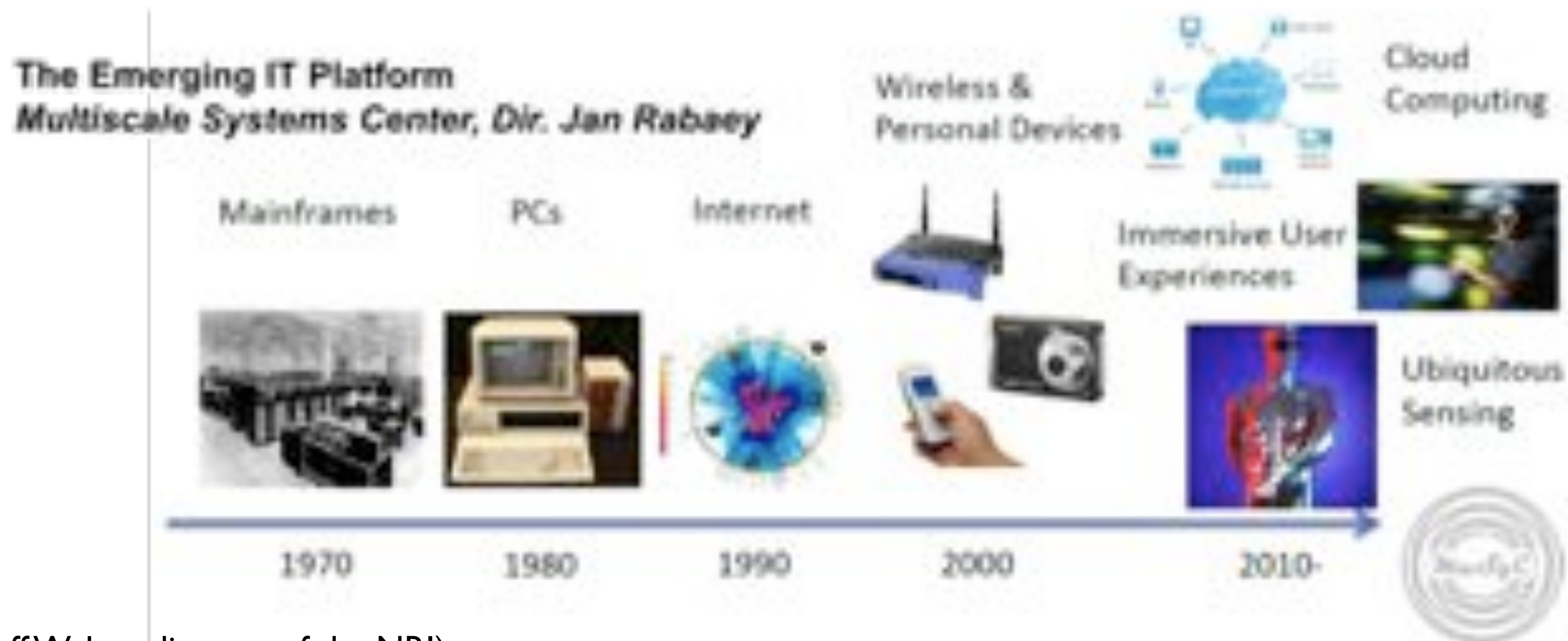


Patrick Stewart and Ian McKellen shared the stage as the leads in Samuel Beckett's "Waiting for Godot"
King's Theatre, Edinburgh, Mon 13–Sat 18 Apr 2011

Vision for the Future (from Jeff Welser, director of the NRI)

"HOW" to Build to "WHAT" to Build!

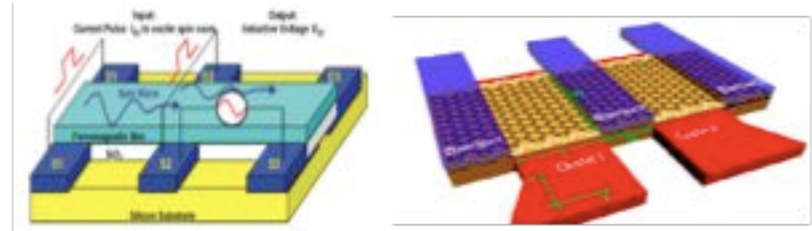
- Barrier to future scaling changing from "how do we make them smaller?" to "how do we reduce power to make them usable?"
  - Change happened between the 100nm and 10nm barriers!
- Many new materials with new physics, properties & functionality.
  - Shift from single device focus to circuits/architecture integration



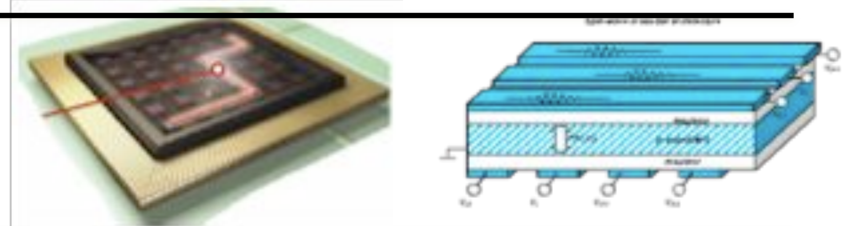
(from Jeff Welser, director of the NRI)

NRI Primary Research Vectors

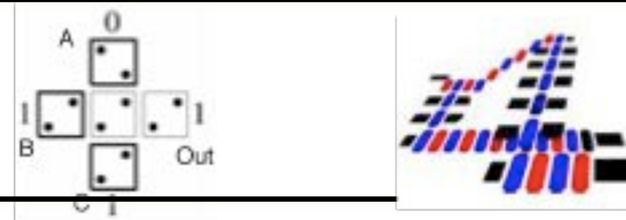
- NEW DEVICE
  Device with alternative state vector



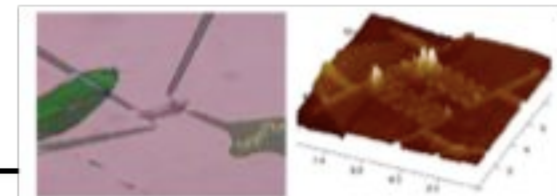
- NEW WAYS TO CONNECT DEVICES
  Non-charge data transfer



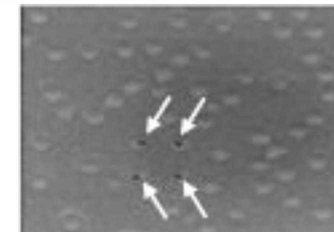
- NEW METHODS FOR COMPUTATION
  Non-equilibrium systems



- NEW METHODS TO MANAGE HEAT
  Nanoscale phonon engineering



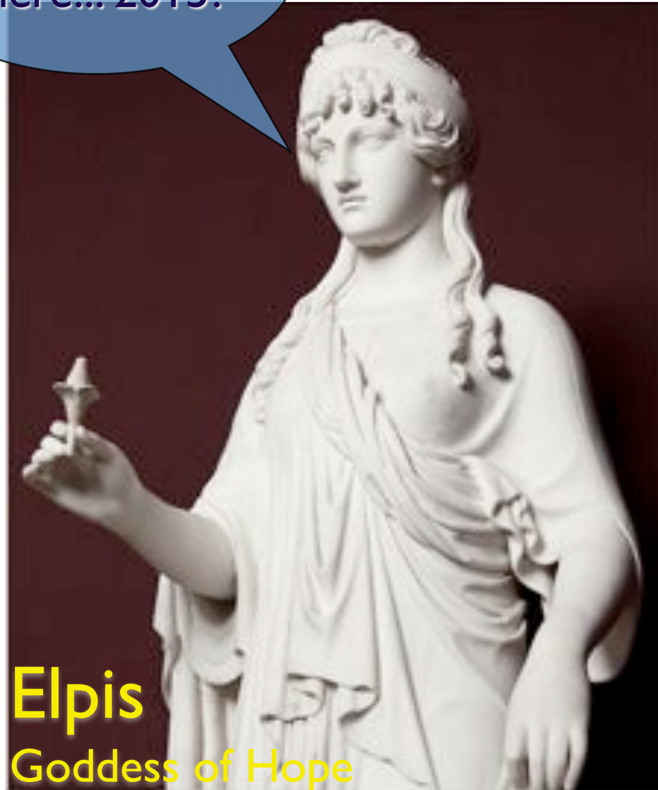
- NEW METHODS OF FABRICATION
  Directed self-assembly devices



(from Jeff Welser, director of the NRI)

But When?

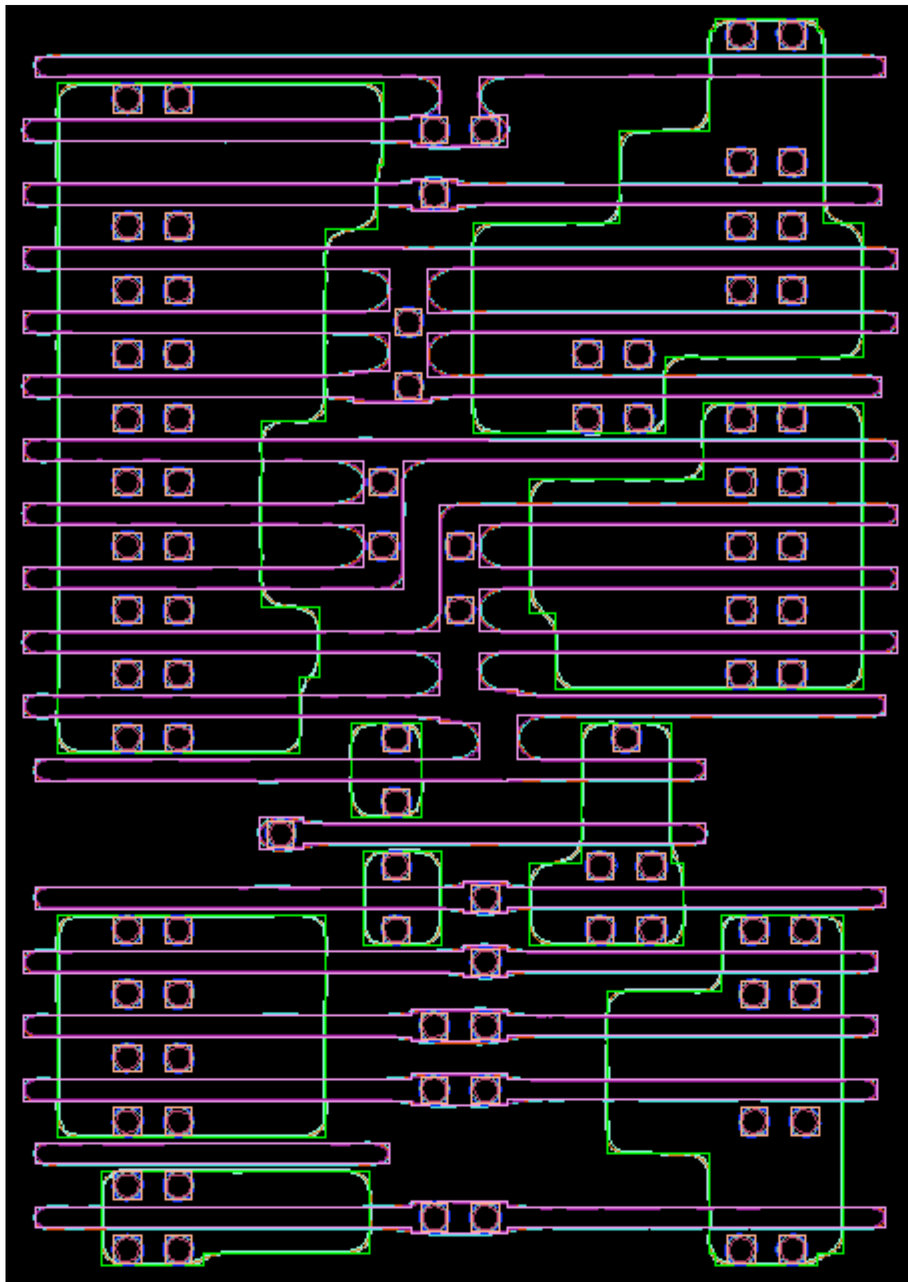
- The only honest answer is “not soon enough”.



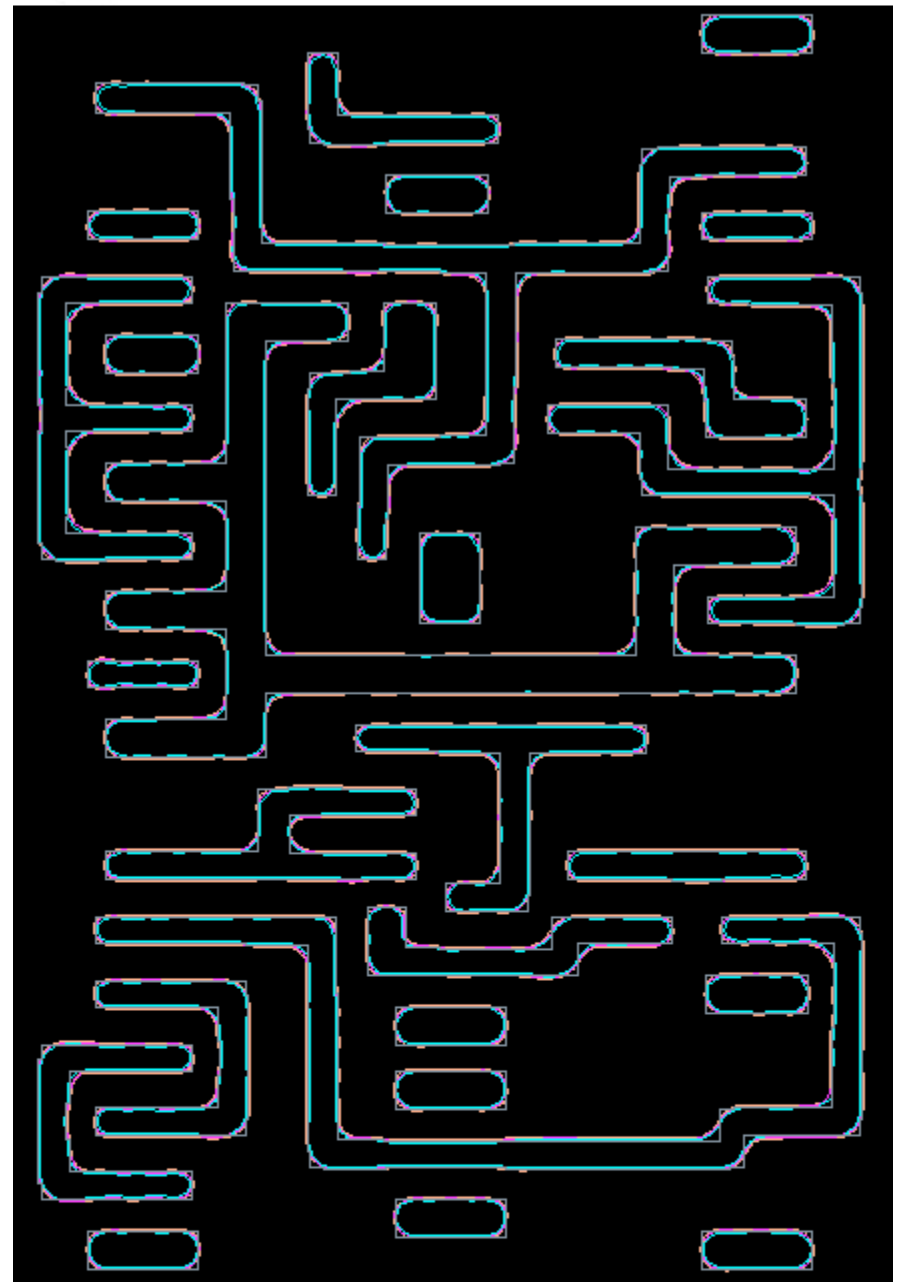
What do we do while Waiting?

- There are a number of problems to overcome:
- Lithography.
  - This is a complex issue, with the uncertainty around UV making things harder. Computational Lithography, Double/ Triple patterning, and layout regularity are all in the mix.
- Power.
  - This will remain a hard problem. While some benefit can come from device and technology improvements, much remains at the software and system levels.
- Resilience.
  - This gets less press time, but is just as hard a problem. We cannot count on 100% functionality any longer!

A Latch in 45nm Technology



Polysilicon, Diffusion, and Via contours



M1 contours

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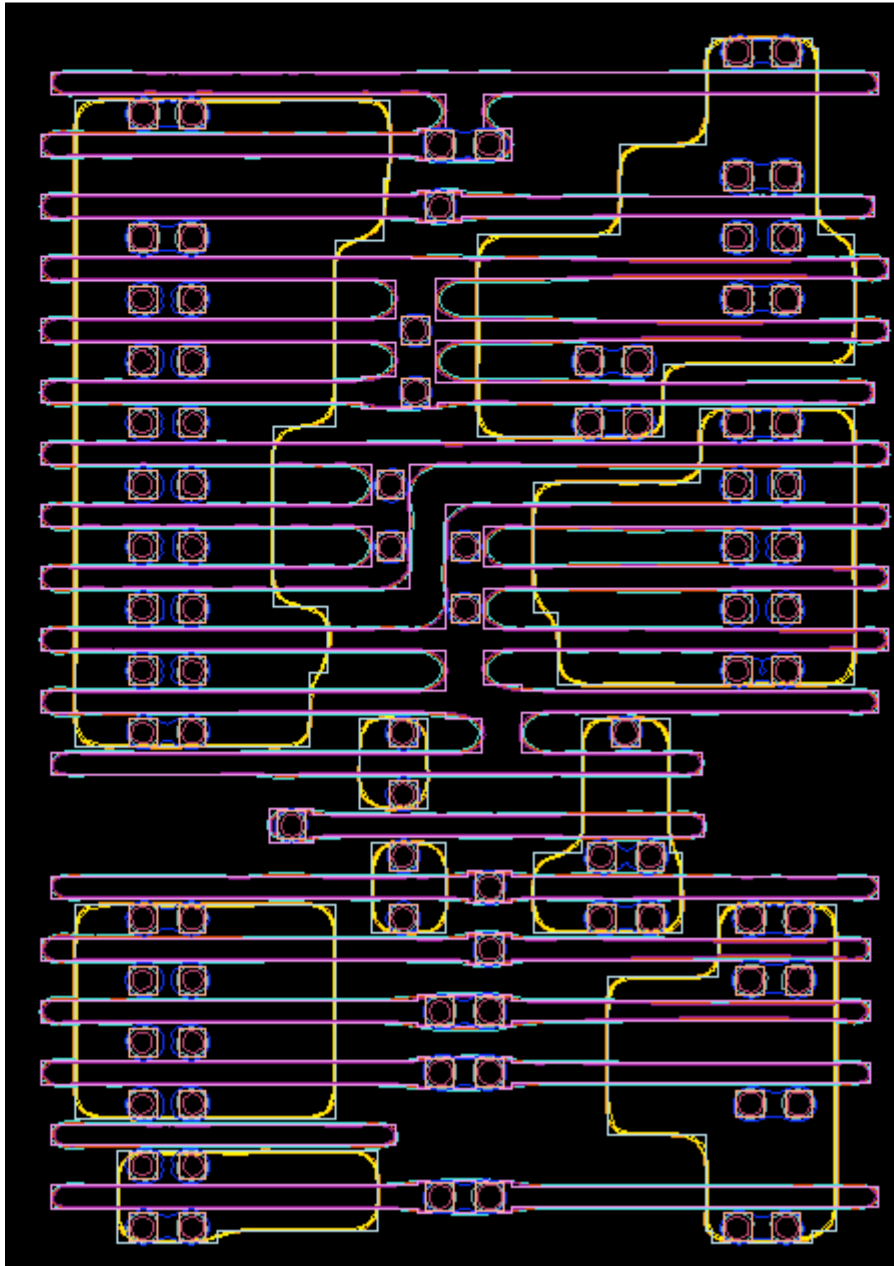
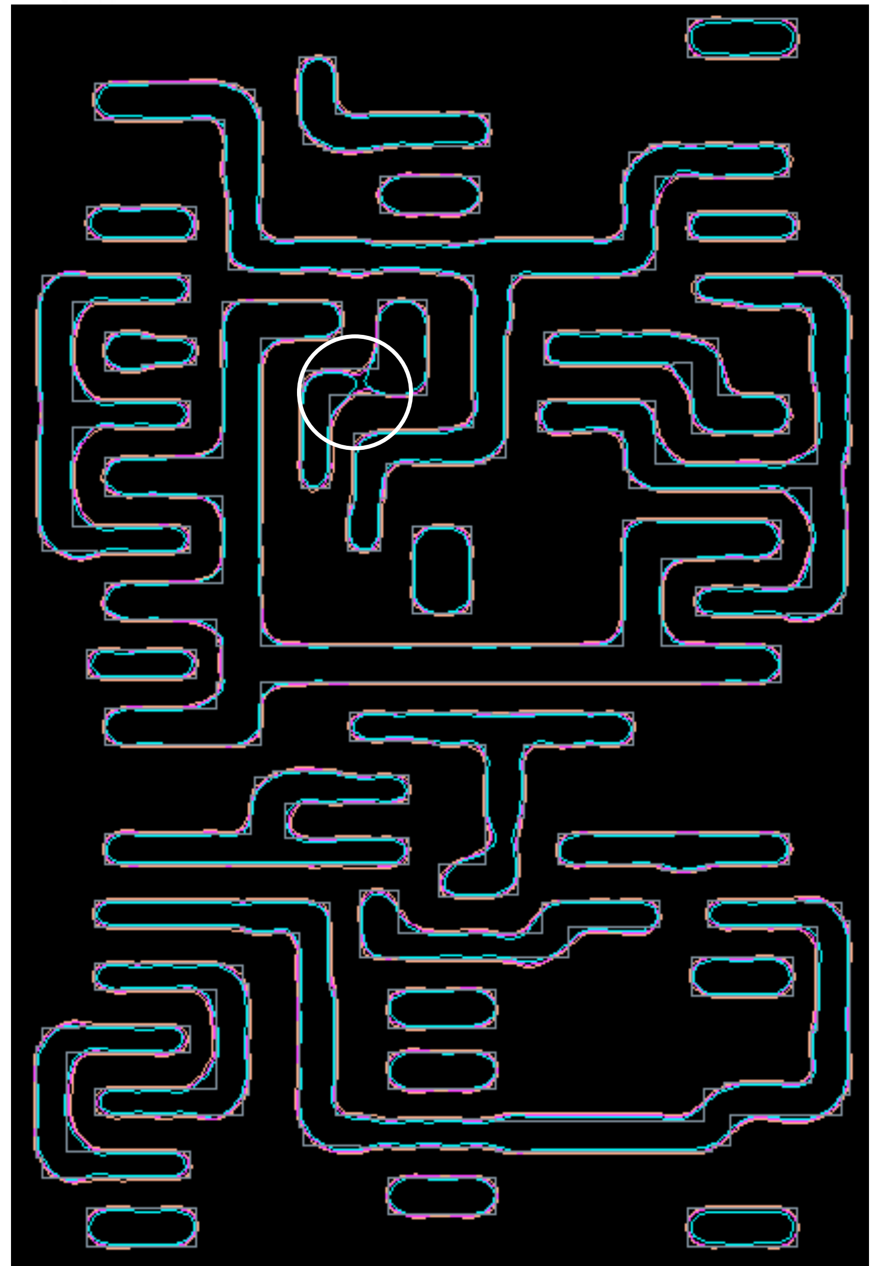
A Latch in 45nm Technology shrunk to 32nm



Polysilicon, Diffusion, and Via contours



M1 contours

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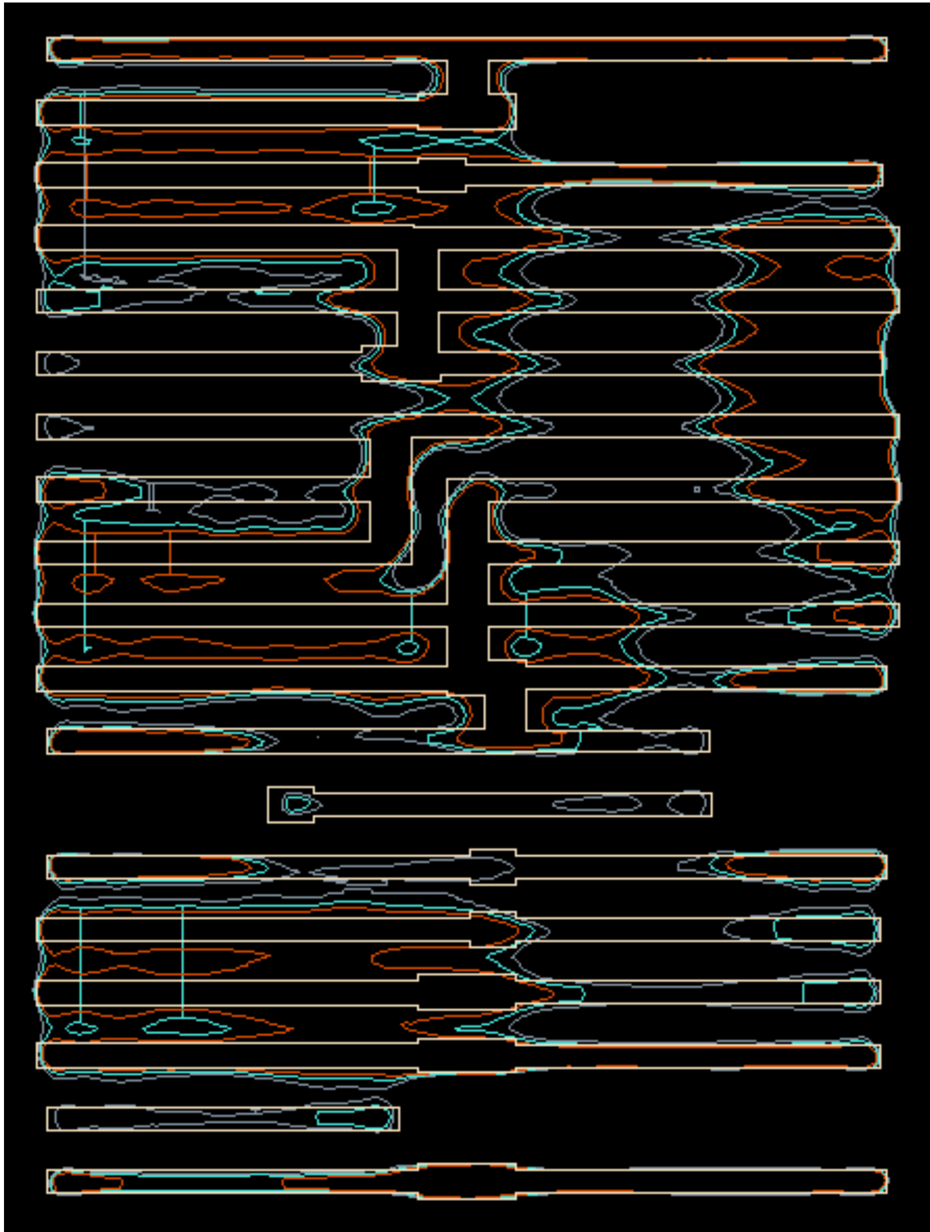
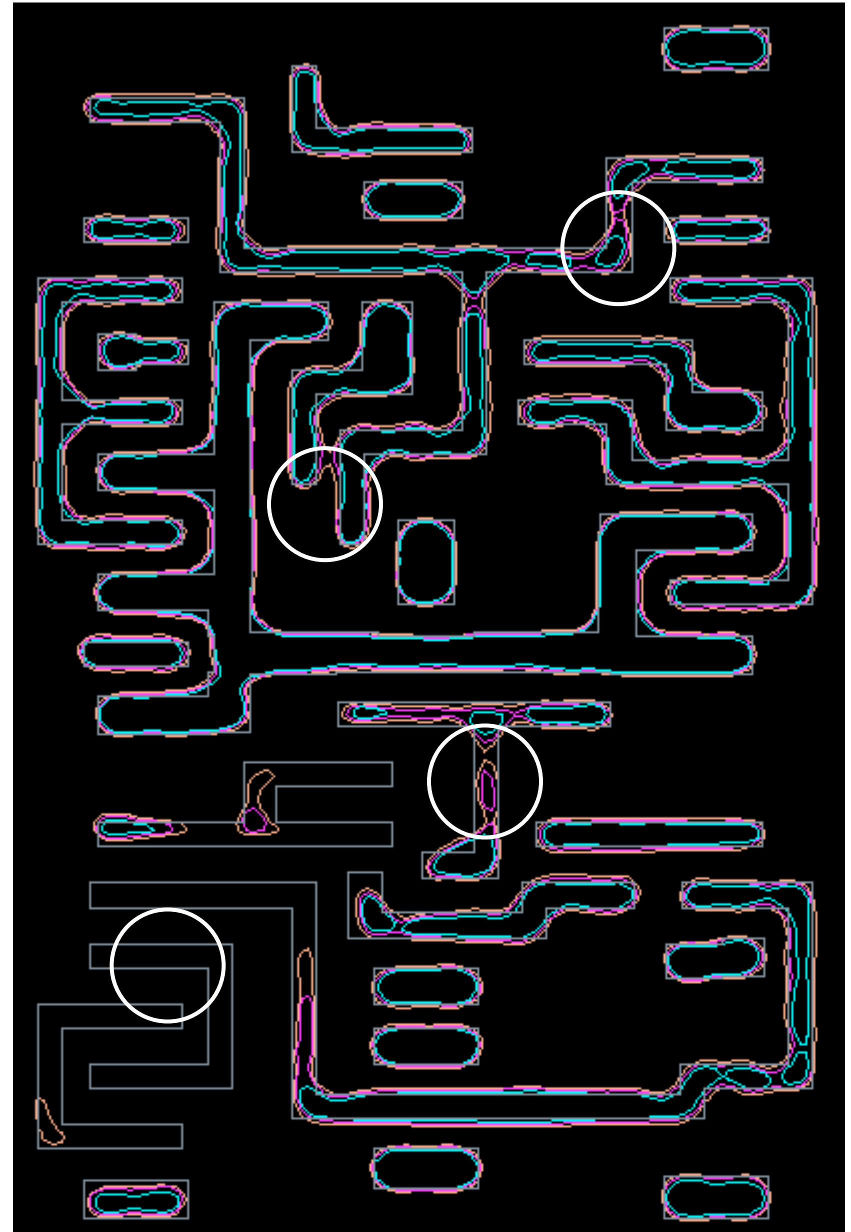
A Latch in 45nm Technology shrunk to 28nm



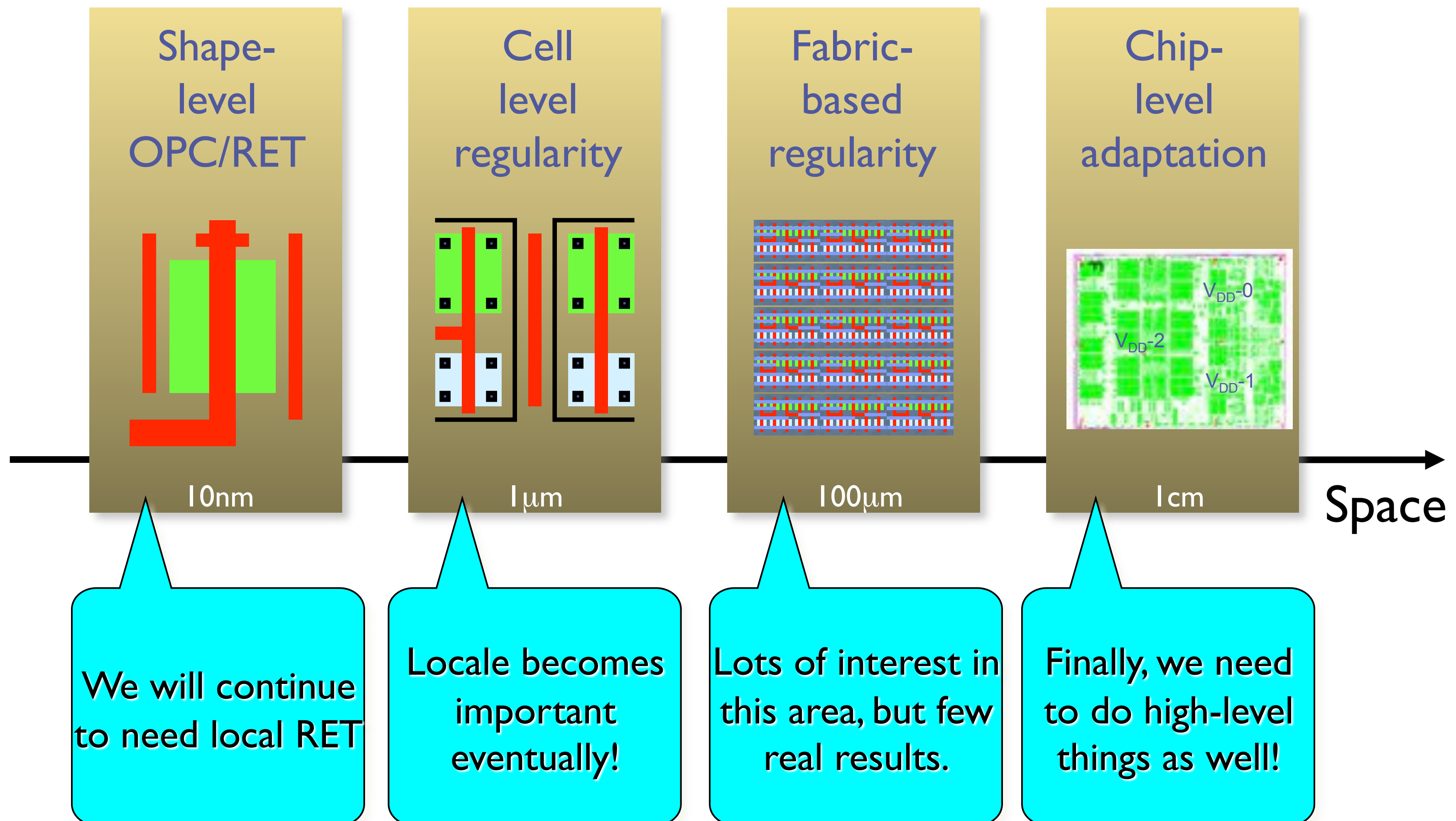
Polysilicon, Diffusion, and Via contours



M1 contours

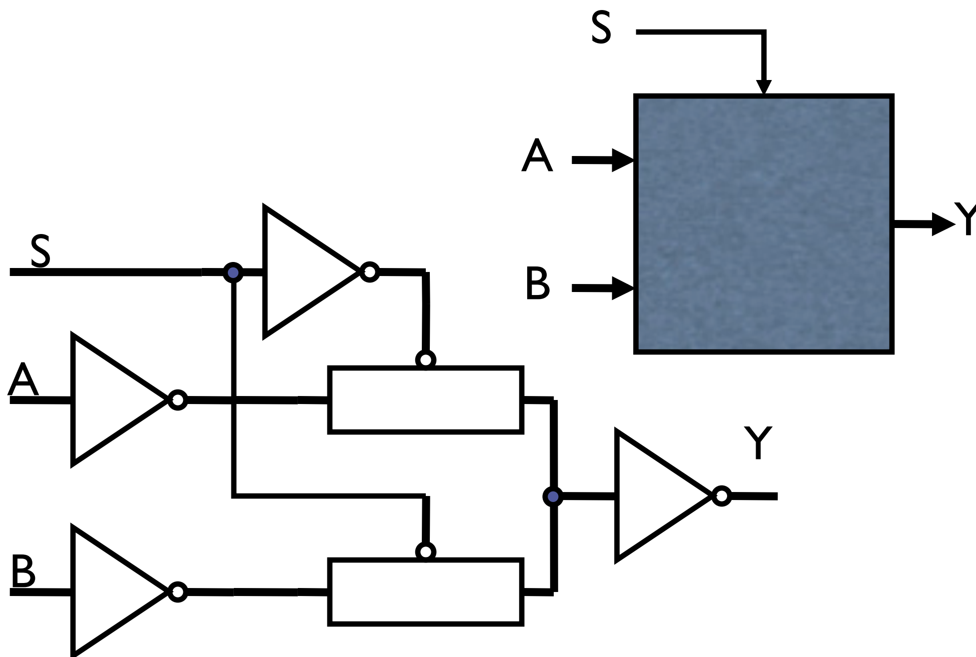
Responses to Lithography Difficulties

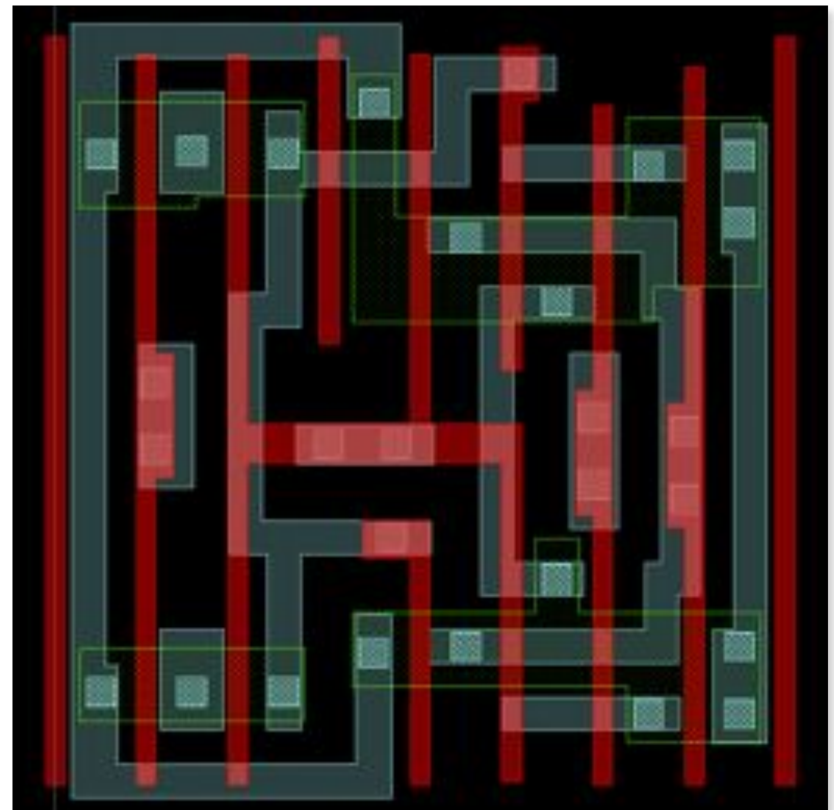
- Responses at different levels of granularity!



Layout Regularity Example

- Two-Input Multiplexer circuit (ARM layout).
  - 45nm library, somewhat dirty layout…
  - Polysilicon, Diffusion and Metal-1 all show some significant "lack of regularity"!





Irregularity

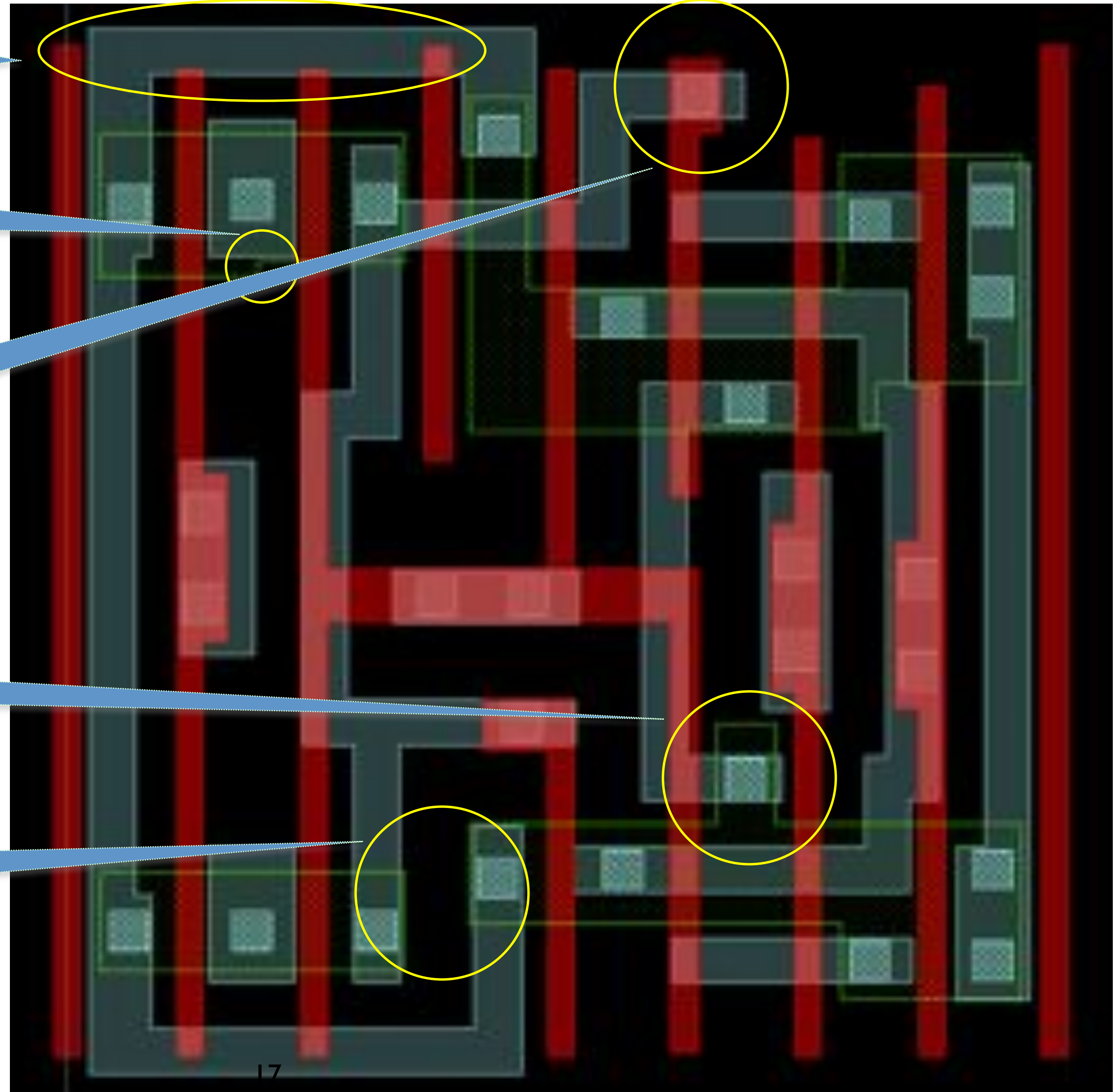
Irregular Polysilicon end

Diffusion Notch

Polysilicon Notch

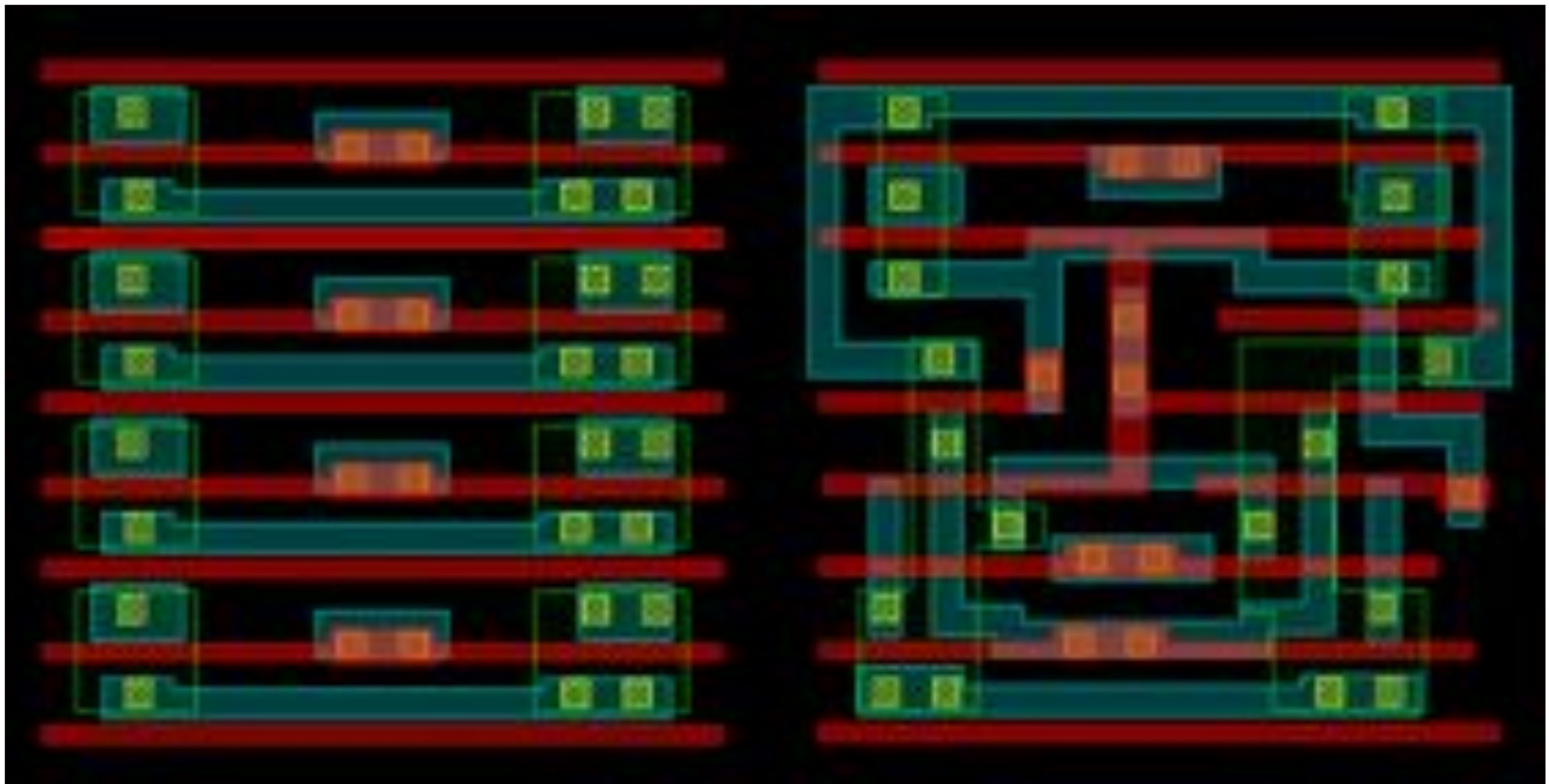
Diffusion Notch

Missing Polysilicon



Clean vs. Dirty Layouts

- 4 inverters vs. Multiplexer. Same area, very different regularity.



Regularity Impact on Circuit

- We analyzed the 4 inverters and the 2-way mux to assess lithography-induced dimensional variability across the standard process window.
  - These results are for 45nm... Expect more for newer

Cell	Best Device σ (nm)	Worst Device σ (nm)	% Difference
INV	2.479	2.514	1.41
MUX2	2.189	2.671	22.02

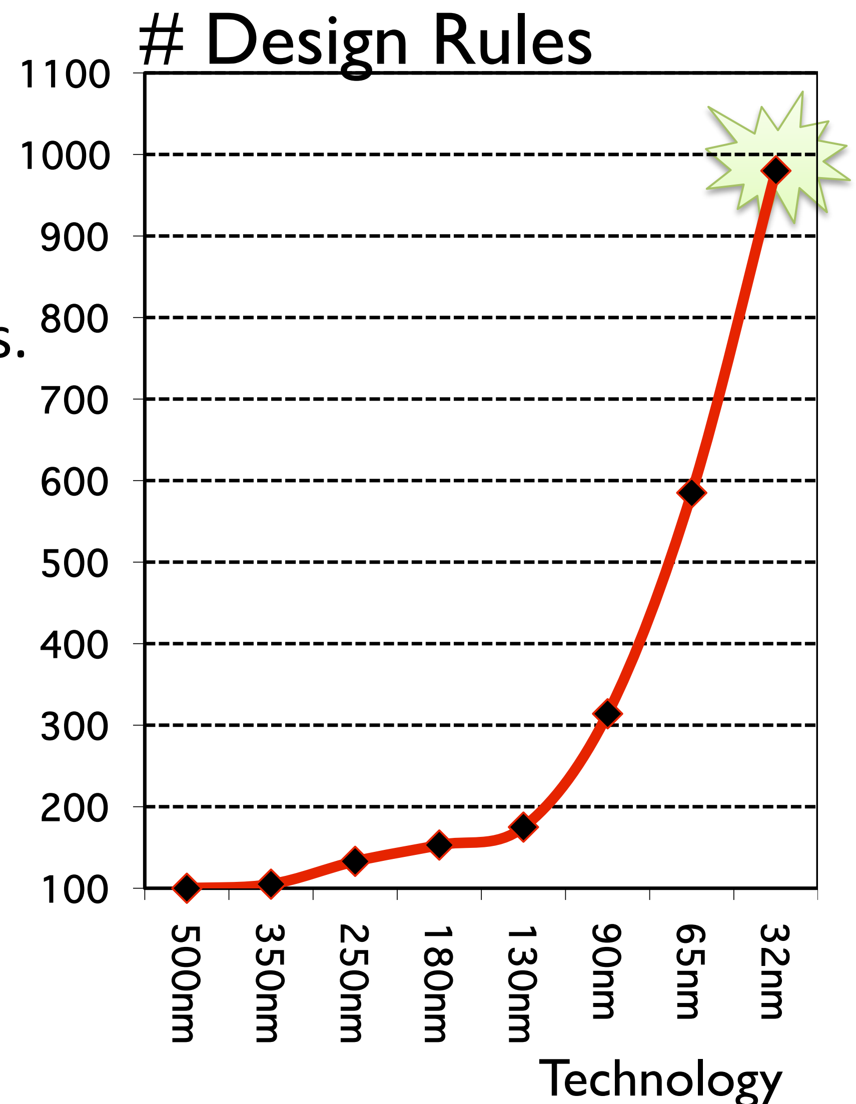
Close

Far

Example of how much layout regularity *might* buy us!

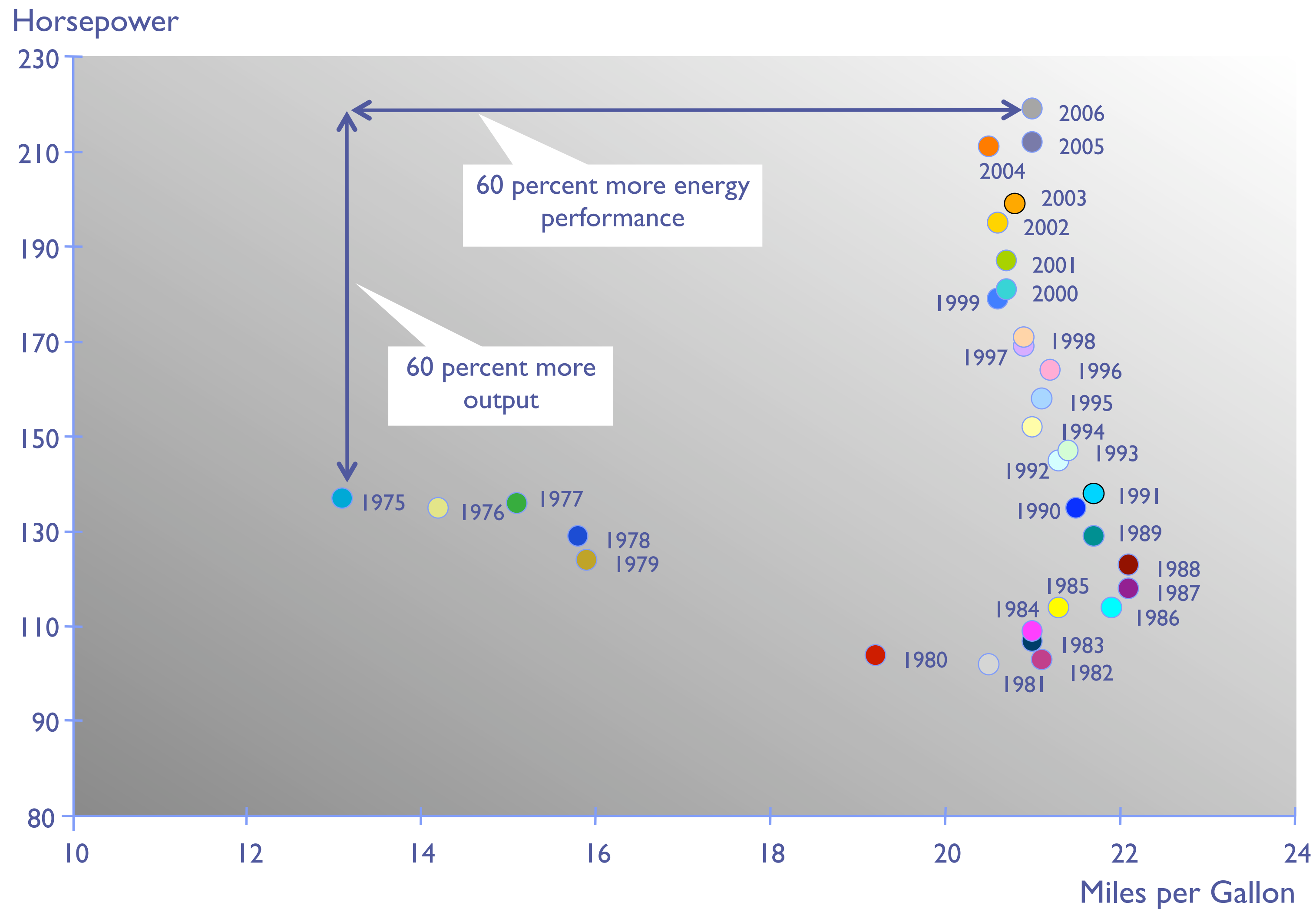
What Should We Do?

- The RMS (**R**ules **M**odels **S**hapes) contract is broken.
  - Cannot legislate better layout with more and more design rules.
- Need better implementation styles that solve this problem without impacting density!
  - And with the same level of automation existing now.
- Why can't this be solved in the context of a cell library?



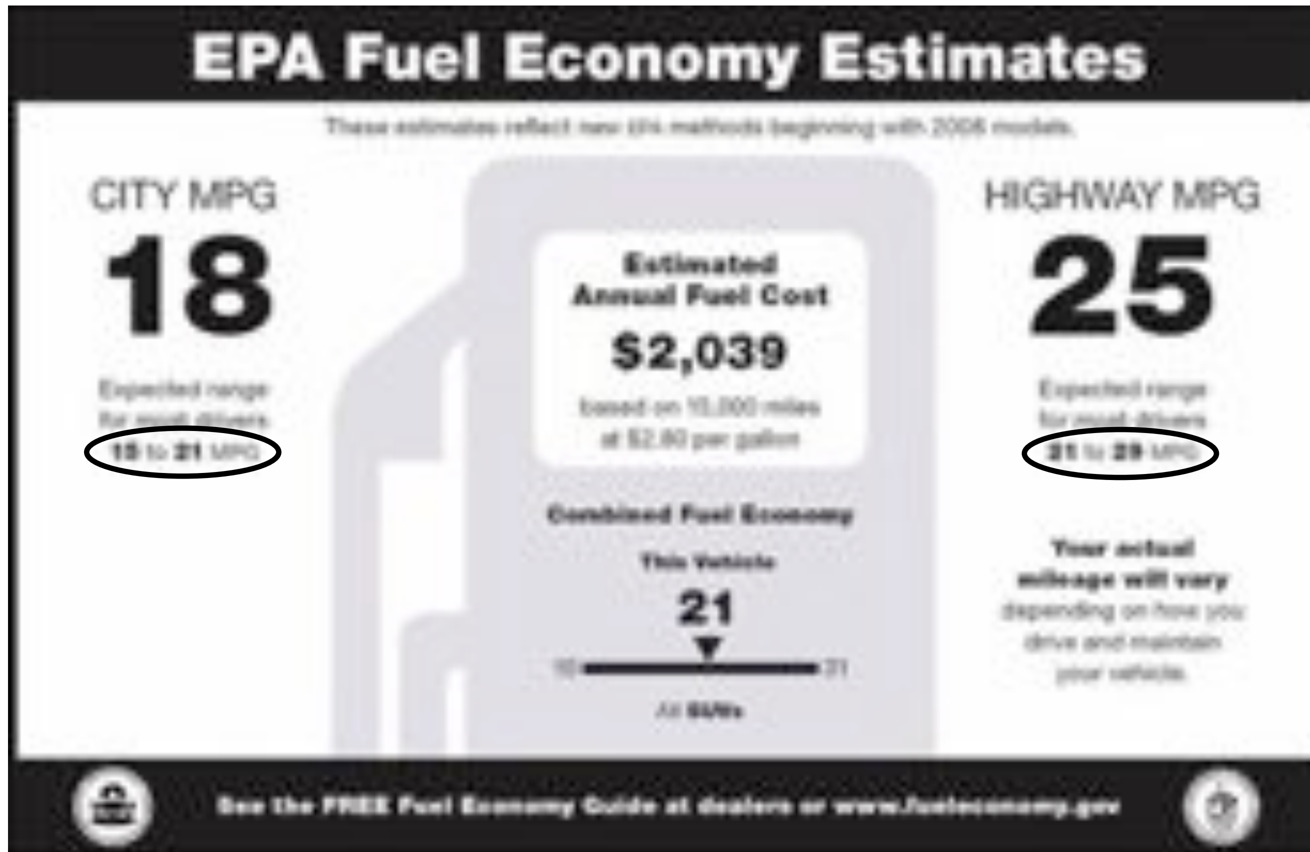
Gas Prices…

R&D Impact on Car Efficiency…



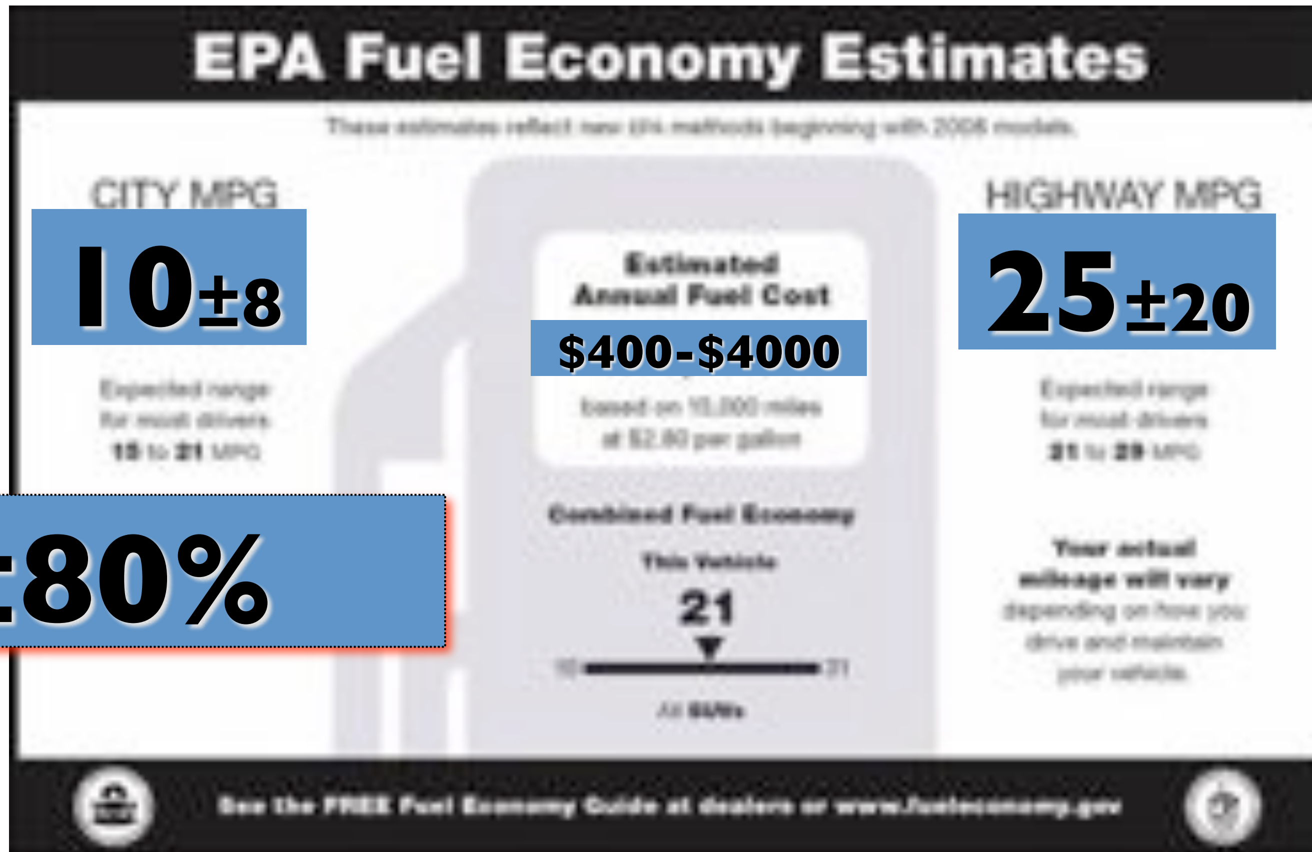
Source: Environmental Protection Agency, Light Duty Automotive Technology and Fuel Economy Trends: 1975-2006, July 2006.

Certainty… A valuable commodity



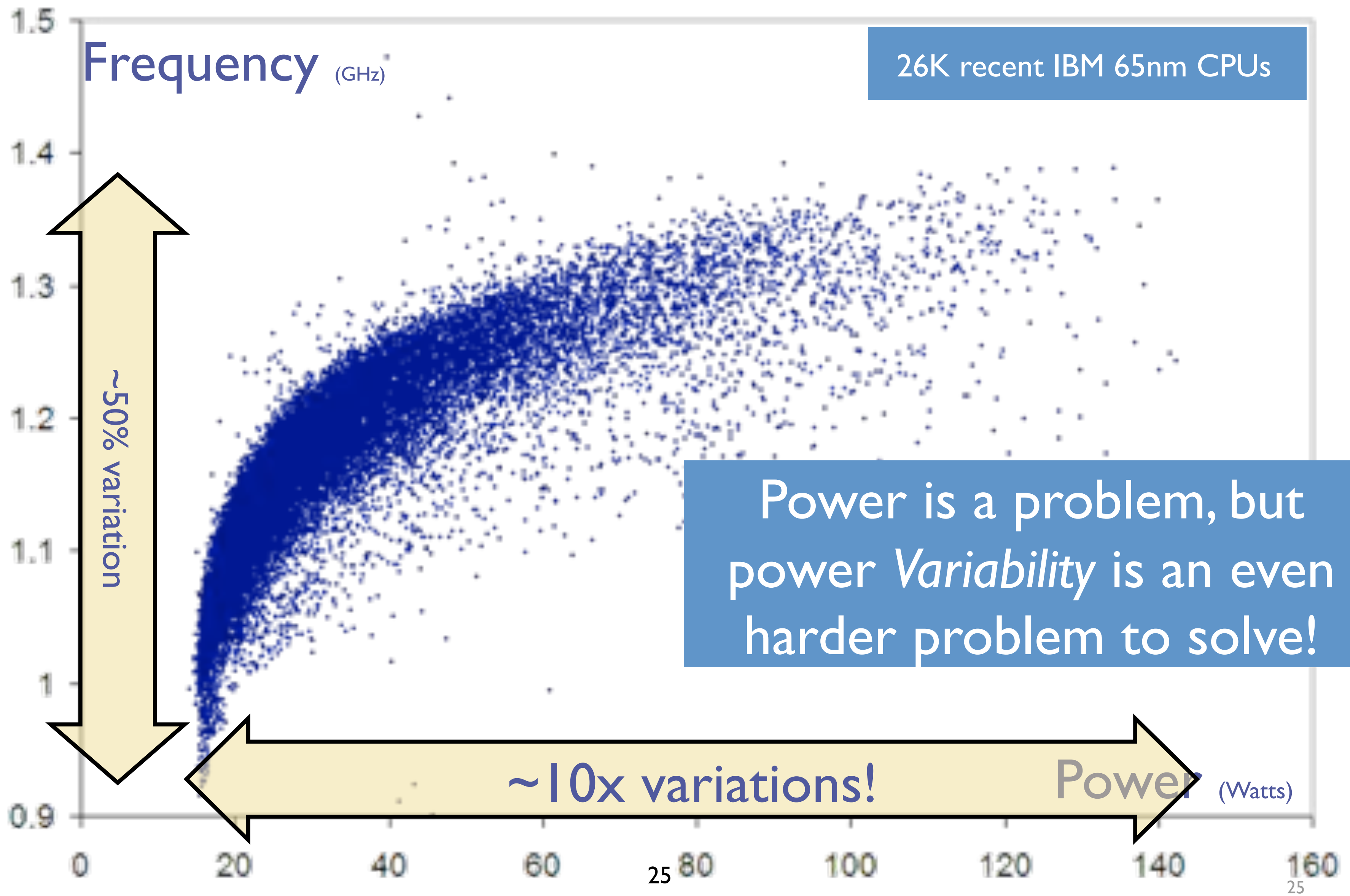
±16%

High Variability = Low Quality?



- Would you buy this car?

Would you buy this chip then?



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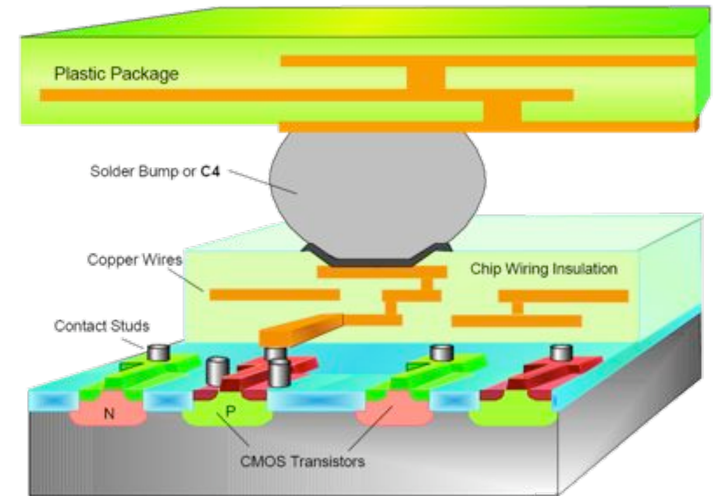
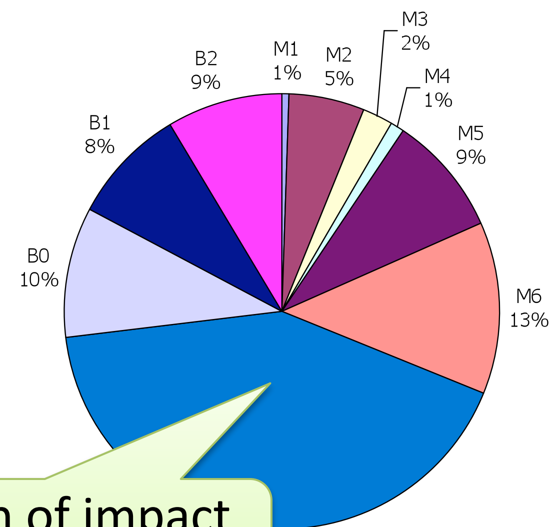
What Should We Do?

- The power estimation problem needs to get solved.
  - And it needs to drive a variability-aware system-level power reduction methodology.
- Linkage between high level power and low level electrical (noise, voltage drop, electro-migration) missing!
- Why isn't there a unified stochastic framework to deal with workload and manufacturing variability?





Resilience and Failure?

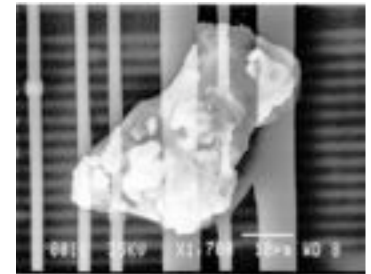
- As we make our systems ever more complex, failure becomes more and more possible.
  - Systems are a mish-mash of software, hardware, sensors, actuators, etc…
- Failure can be because of external factors (noise), aging (metal fatigue) or design (a bug).

Charles Babbage's "Difference Engine"

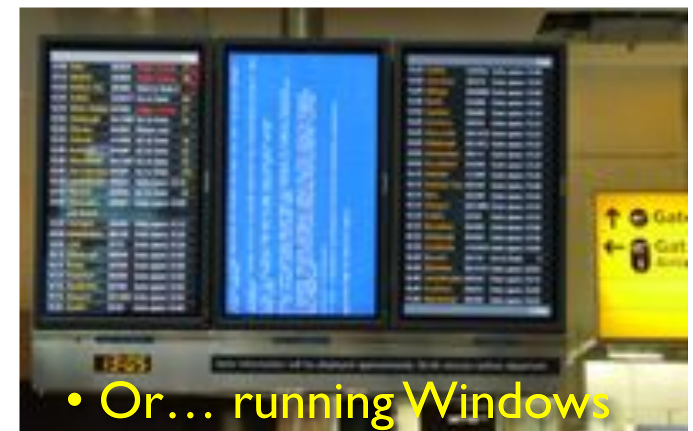
- As scaling slows down, with no post-Si technology available yet, we have no choice but to continue pushing present technology.
  - And many have stopped scaling and pushing...
- We are at the beginning of a discontinuity in failure rates of semiconductor systems!

Failures Types

- Failures in integrated circuits can be of two varieties:
- HARD failures are characterized by a permanent mismatch between expected and observed behavior.
  - An output is stuck at 0 or 1!
  - Cause: often a topological change.



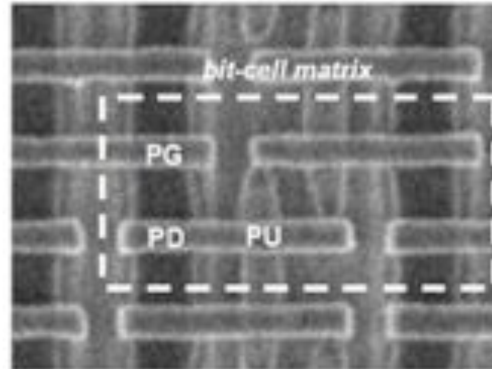
- SOFT failures occur occasionally or under a specific set of conditions.
  - Excessive power at high T.
  - Cause: often a mismatch between models and reality.

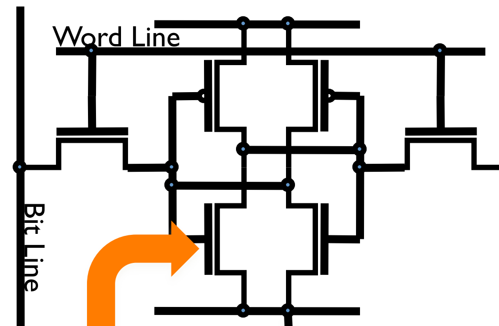


Soft vs. Hard Example: SRAM

Soft

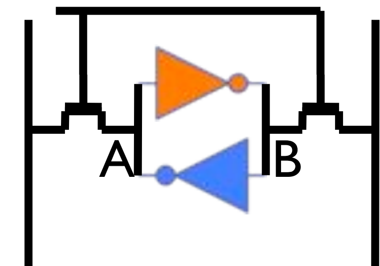
- SRAM cell not able to pull bit line low fast enough to meet access time requirements.
- Perhaps for low V_{DD} only.

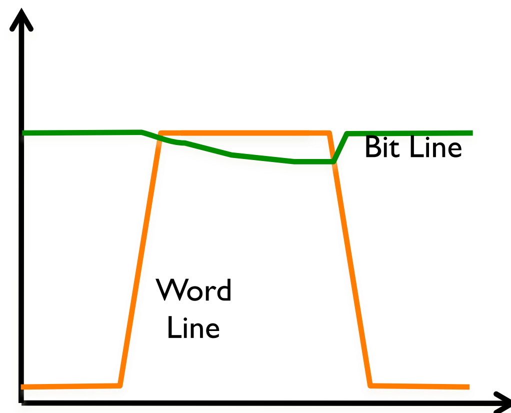


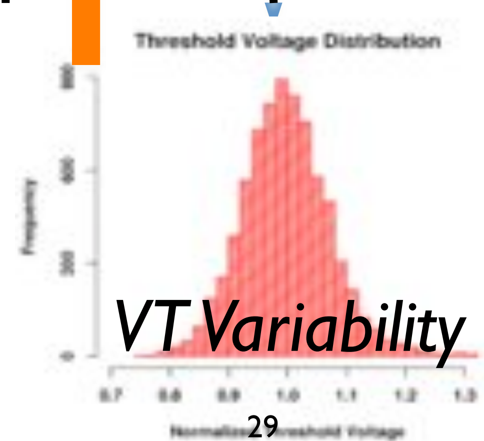


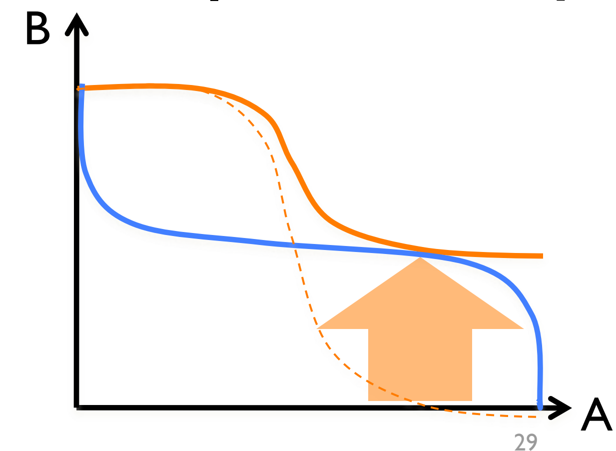
Hard

- SRAM cell so asymmetric that it cannot store a "1".









SRAM Observations

- Since SRAM is a uniform fabric, it is able to "push" the design rules to get higher density.
  - The benefit of regularity and obsessive engineering.

Alternative Regularity

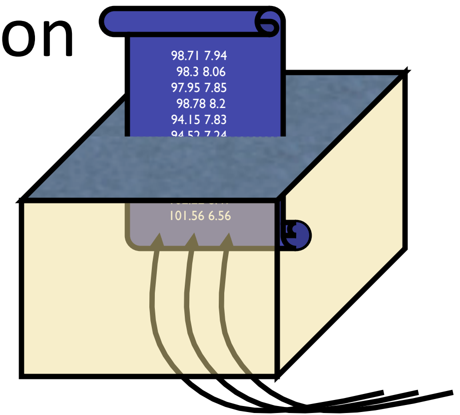
- The price for higher density is <u>higher variability</u>.
  - So high, that SRAM cells can have "catastrophic" failure, e.g. cell loses data when we read it.
- The solutions are:
  - Add redundancy and error correction at the architecture level.
  - Aggressively predict and manage the electrical design margins for SRAM at the circuit/device levels.

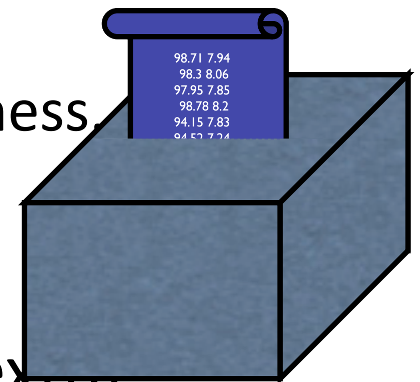
Introduction to Variability

- Variability means lack of uniformity.
  - Individual devices are NOT identical.
  - Individual chips are NOT identical.
- Fluctuations imply unpredictability, which ultimately leads to un-profitability (and the perception of low quality).
  - Sales team needs a predictable product to spec!
- Variability increasing with technology scaling.
- Variability can be systematic or random.
  - Design dependent, or imposed upon design...

Random vs. Systematic?

- Systematic variability occurs when variation is caused by a known phenomena.
  - Location: Wafer edge different from center!
  - Implementation: Layout dependence!
- Random variability occurs when the law of large numbers fails, i.e. for atomistic phenomena driven by scaling.
  - Random dopant fluctuations, line edge roughness,
  - Exacerbated for smaller devices.
- Systematic variability can be nulled out by the designer, random variability requires extra design margin and cost! - Difference: knowledge…





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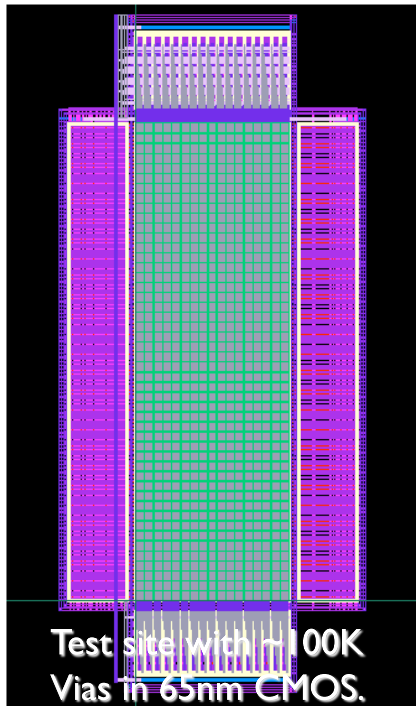
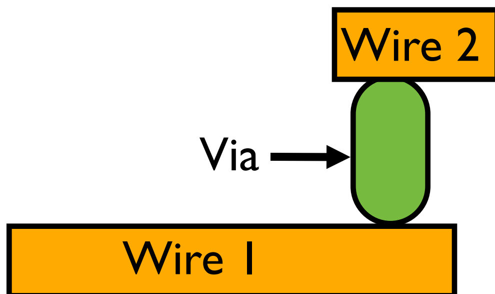
Systematic Variability Example: Vias





Double vias appear to behave fairly consistently

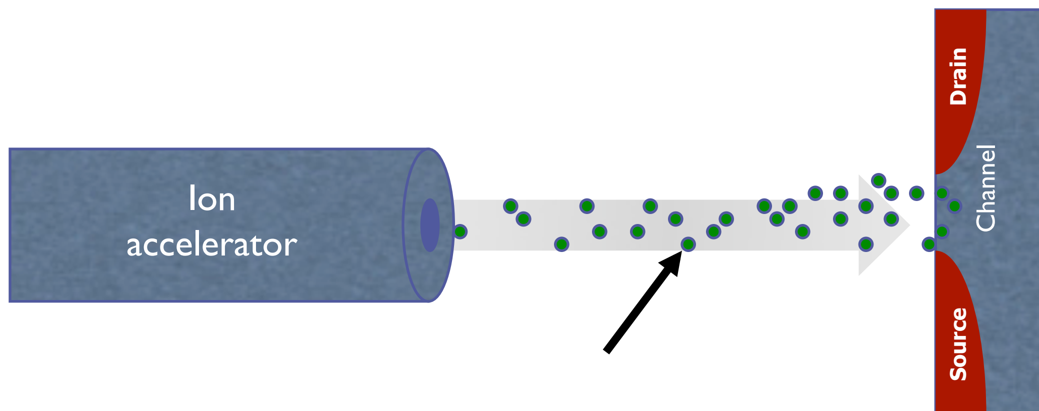
Single vias exhibit high and systematic variability

Systematic need not imply "deterministic".

Via Resistance

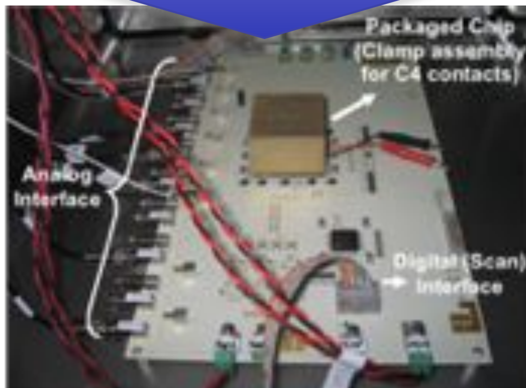
Random Variability

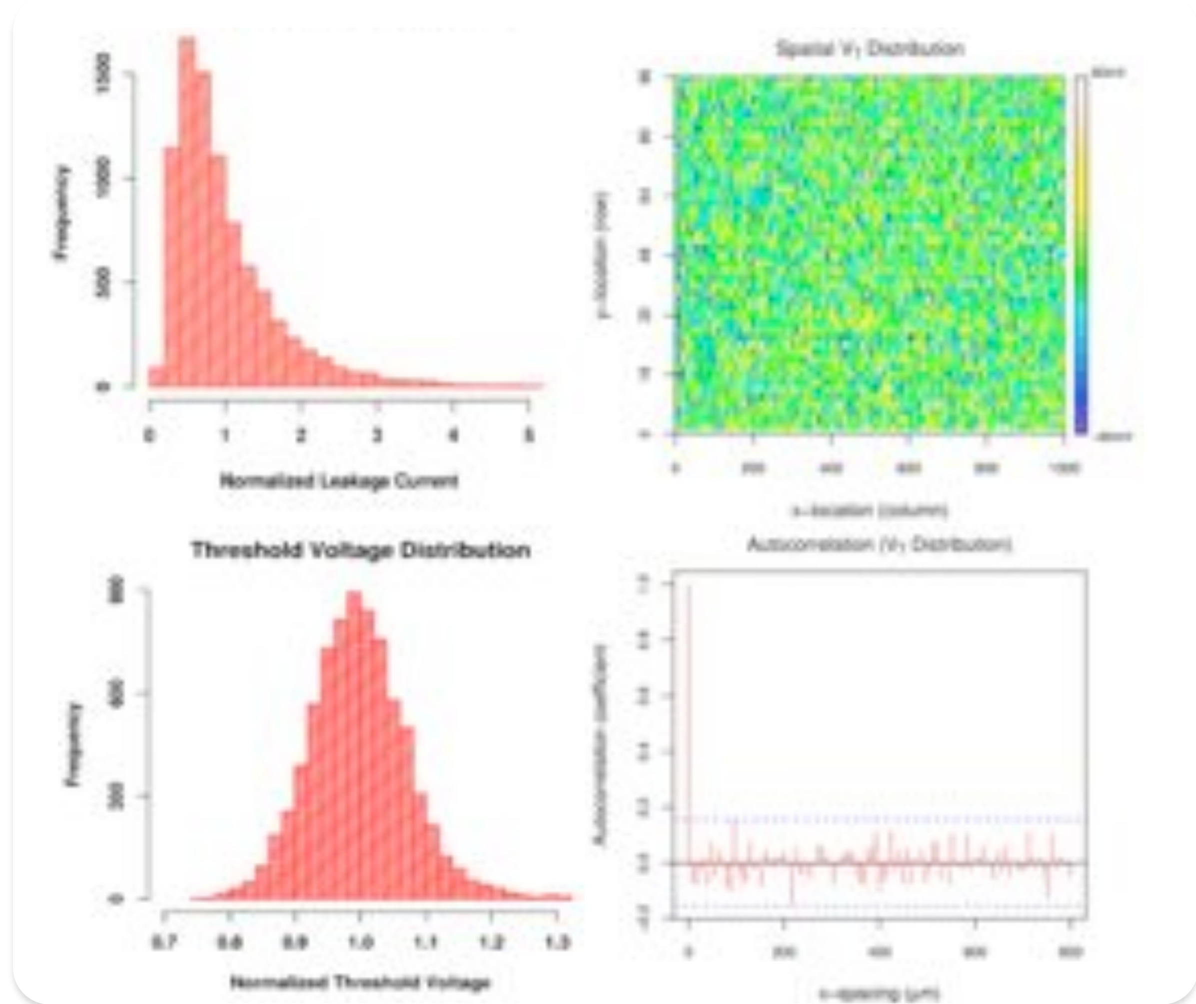
- In modern devices, the channel is very very small and the number of dopant atoms is countable (~50).
  - The location of individual atoms matters!
  - But the process of inserting these atoms (ion implantation) is essentially random!
- So… in modern MOSFETs, the doping of the channel is random and no systematic model exists.
  - Primary impact: threshold voltage variations!



Random Variability in MOSFETs

Test site with 100K devices in 65nm SOI (SRAM-sized)



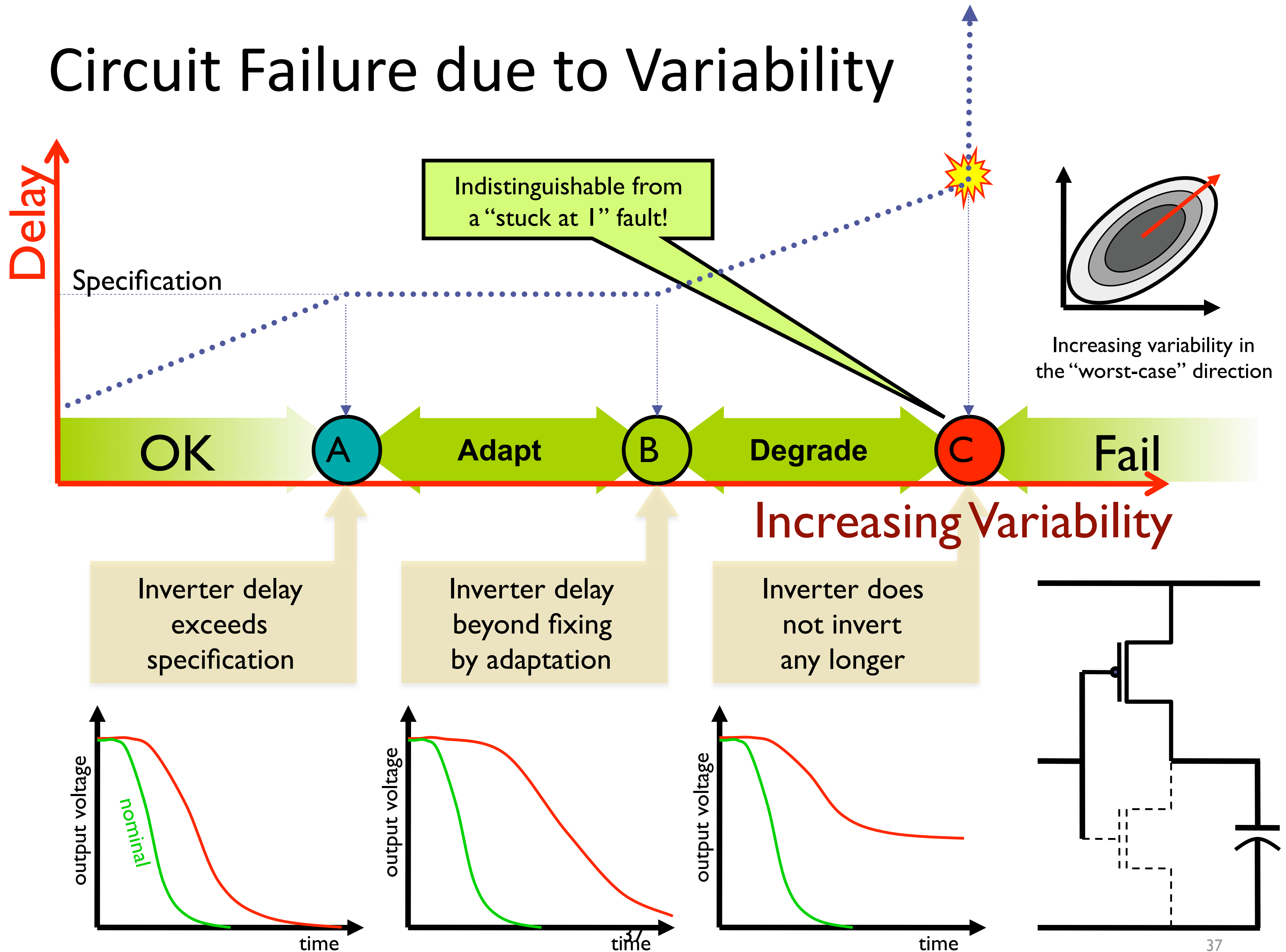


Parameter Distributions   Spatial Correlation

Current Research on Variability

- Much current work is focused on the short term impact.
  - Examples: SSTA, SRAM analysis, Analog circuit yields, etc…
- Impact of increasing variability will change in character!
  - And will need to be handled at higher levels of design!
- 1st order impact: delay and power variability (at 90nm).
  - Widely published, numerous EDA tools available.
- 2nd order impact: reliability of devices and wires (at 45nm).
  - Less widely published, more open problems (e.g. EM).
- 3rd order impact: resilience (at 22nm).
  - Emerging currently –little published work!

Circuit Failure due to Variability

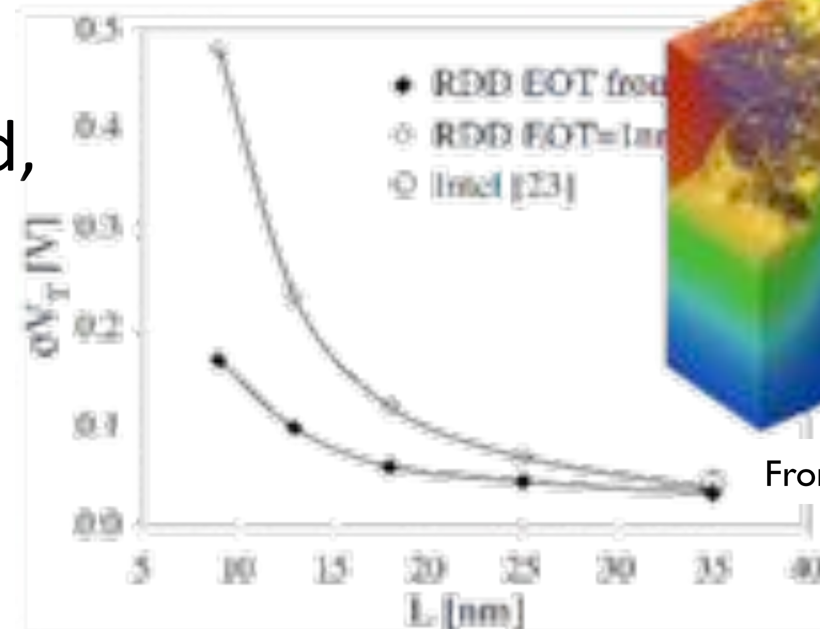


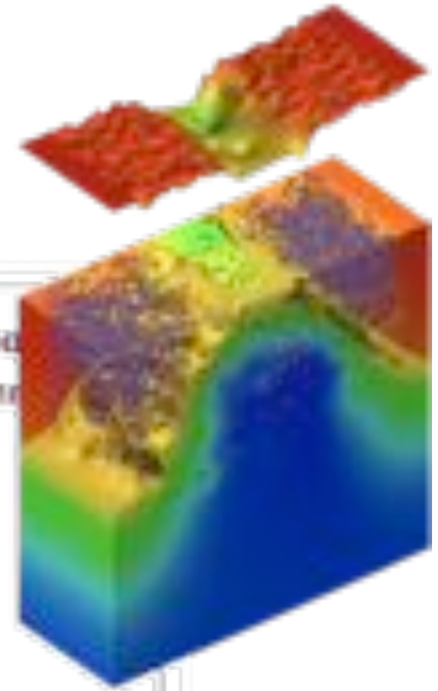
Recent Results (part of ITRS'10)

Part of a "resilience roadmap" being developed (DATE'10).

What Should We Do?

- There are be some technology fixes (like FDSOI) that can help a little, but increasing variability will impact circuit operation/correctness.
- How can we do for the whole system what we have already done for SRAM?
- It must be automated, and it must be verifiable!





From Prof. Asenov

Conclusions

- We need to keep Si/CMOS going for the foreseeable future.
  - This will require solving significant challenges in lithography, power and resilience ... At the same time that R&D investment in this area is reducing because of consolidation.
- Failure rates for circuits from Age, Noise and Variability are predicted to become significantly worse with scaling.
  - For some domains (e.g. SRAM) this has been recognized and substantially solved. For other domains, work is needed.
- Fix: innovation at the device, circuit, architecture, system and software levels (example: FDSOI, with no RDF).
  - All levels of the design abstractions stack must co-operate in order to solve the problem.
  - We must sustain Si until the “post” technology arrives.