Thursday

	Session A - Room 351	Session B - Room 343
8:30	**Opening Session - Room 351**	
9:00	**Joint Keynote - Grand Ampitheater, Level 1**	
10:30	**Coffee Break**	
	Test 1 - Room 351 *Session Chair - Emre Salman, Stony Brook University, USA*	**Low Power - Room 343** *Session Chair - Jeff Draper, University of Southern California, USA*
10:45	**A novel statistical and circuit based technique for counterfeit detection in existing ICs** Rashmi Moudgil; Dinesh Ganta; Leyla Nazhandali; Michael Hsiao; Simin Hall; Chao Wang *Virginia Tech, USA*	**Harvesting-Aware Energy Management for Multicore Platforms with Hybrid Energy Storage** Yi Xiang; Sudeep Pasricha *Colorado State University, USA*
11:10	**Unexcitability Analysis of SEUs Affecting the Routing Structure of SRAM-based FPGAs** Cinzia Bernardeschi; Luca Cassano; Andrea Domenici; Luca Sterpone *Università di Pisa, Italy; Politecnico di Torino, Italy*	**Early Stage Power Management for 3D FPGAs Considering Hierarchical Routing Resources** Krishna Chaitanya Nunna; Farhad Mehdipour; Kazuaki Murakami *Kyushu University, Japan*
11:35	**A Novel Intermittent Fault Markov Model for Deep Sub-Micron Processors** Babak Saghaie; Roshan Ragel; Sri Parameswaran; Aleks Ignjatovic *The University of New South Wales, Australia*	**A Low power 6T-SRAM using negative bit-line for variability tolerance beyond 22nm node** Pablo Royer; Marisa Lopez-Vallejo *Universidad Politécnica de Madrid, Spain*
12:00	**High-Endurance Hybrid Cache Design in CMP Architecture with Cache Partitioning and Access-Aware Policy** Shun-Ming Syu; Ing-Chao Lin; Yu-Hui Shao *National Cheng Kung University, Taiwan*	**Virtual Register Renaming: Energy Efficient Substrate for Continual Flow Pipelines** Komal Jothi; Haitham Akkary *American University of Beirut, Lebanon*
12:15	**Lunch - Defy/Derian Rooms, Level 2**	
	Best Paper Session - Room 351 *Session Chair - Patrick Madden, SUNY Binghamton, USA*	
13:30	**Skew-Bounded Low Swing Clock Tree Optimization** Can Sitik; Baris Taskin *Drexel University, USA*	
14:00	**Coordinating Prefetching and STT-RAM based Last-level Cache Management for Multicore Systems** Mengjie Mao; Hai Li; Alex K. Jones; Yiran Chen *University of Pittsburgh, USA*	
14:30	**Variability-Aware Design of Energy-Delay Optimal Linear Pipelines Operating in the Near-Threshold Regime and Above** Qing Xie; Yanzhi Wang; Massoud Pedram *University of Southern California, USA*	
15:00	**Coffee Break - Corridor, Level 3**	
	VLSI Circuits - Room 351 *Session Chair - Fabrizio Lombardi - Northeastern University, USA*	**CAD 1 - Room 343** *Session Chair - Erik Brunvand, University of Utah, USA*
15:15	**An Energy-Efficient Truly All-Digital Temperature Sensor for SoC Applications** Tzu-Yuan Kuo; Keng-Jui Chang; Jen-Hsiang Lee; Zong-Wu He; Jinn-Shyan Wang *National Chung-Cheng University, Taiwan*	**GPU Implementation of a Scalable Non-Linear Congruential Generator for Cryptography Applications** Aditya Belsare; Steve Liu; Sunil Khatri *Texas A&M University, USA*
15:40	**Efficient Characterization of TSV-to-Transistor Noise Coupling in 3D ICs** Hailang Wang; Mohammad Asgari; Emre Salman *Stony Brook University, USA; Columbia University, USA*	**Fast and Memory-Efficient GPU Implementations of Krylov Subspace Methods for Efficient Power Grid Analysis** Takumi Morishita; Hiroshi Tsutsui; Hiroyuki Ochi; Takashi Sato *Kyoto University, Japan*
16:05	**A Portable High-Frequency Digitally Controlled Oscillator (DCO)** Muhammad Elrabaa *KFUPM, Saudi Arabia*	**Translation Validation of Scheduling in High Level Synthesis** Tun Li; Yang Guo; Wanwei Liu; Mingsheng Tang *National University of Defense Technology, China*
16:20	**A 250mV Sub-threshold Asynchronous 8051 Microcontroller with a Novel 16T SRAM Cell for Improved Performance in 40nm CMOS** Jaeyoung Kim; Kwen-Siong Chong; Joseph S. Chang; Pinaki Mazumder *University of Michigan, USA; Nanyang Technological University, Singapore*	**LASER - Layout-aware Analog Synthesis Environment on Laker** Yu-Ching Liao; Yen-Lung Chen; Xian-Ting Cai; Chien-Nan Liu; Tai-Chen Chen *National Central University, Taiwan*
16:35	**Poster Session 1 - Corridor, Level 3**	
	VLSI for Biology - Room 351 *Session Chair - Laleh Behjat - University of Calgary, Canada*	**Emerging Technologies - Room 343** *Session Chair - Pinaki Mazumder, University of Michigan, USA*
17:05	**Hardware Acceleration for Retinal Blood Vasculature Segmentation** Dimitris Koukounis; Christos Ttofis; Theocharis Theocharidis *University of Cyprus, Cyprus*	**A New Ternary CNTFET-based Cell with Balanced Memory Operation** Fabrizio Lombardi; Cho Geunho *Northeastern University, USA*
17:30	**A 191μW BPSK Demodulator for Data and Power Telemetry in Biomedical Implants** Li-Lan Wang; Chia-Hsiang Yang; Herming Chiueh *National Chiao Tung University, Taiwan*	**Variability Evaluation of Feedback Circuits Used in Nanoelectronic Memristive/CMOS Circuits** Arne Heittmann; Tobias G. Noll *RWTH Aachen University, Germany*
17:45	**Custom Memory Architecture for Multi-Core Implementation of Face Detection Algorithm** David Watson; Ali Ahmadinia; Gordon Morison; Tom Buggy *Glasgow Caledonian University, UK*	**Asymmetric-access Aware Optimization for STT-RAM Caches with Process Variations** Yi Zhou; Chao Zhang; Guangyu Sun *Beijing Institute of Technology, China; Peking University, China*
18:00	**Break**	
18:30	**Reception - Espace Renoir, Le Meridien Etoile hotel**	

Friday

	Session A - Room 351	Session B - Room 343
9:00	**Joint Keynote - Amphitheater Bordeaux, Level 3**	
10:30	**Coffee Break**	
	VLSI Design 1 - Room 351 *Session Chair - Dirk Stroobandt - University Ghent, Belgium*	**CAD 2 - Room 343** *Session Chair - Shuai Wang, Nanjing University, China*
10:45	**A New Extension Method of Retention Time for Memory Cell on Dynamic Random Access Memory** Yoshiro Riho; Kazuo Nakazato *Nagoya University, Japan*	**Scaling RTL Property Checking Using Feasible Path Analysis and Decomposition** Lingyi Liu; Shobha Vasudevan *University of Illinois at Urbana-Champaign, USA*
11:10	**A Hardware-Oriented Dynamically Adaptive Disparity Estimation Algorithm and its Real-Time Hardware** Abdulkadir Akin; Ipek Baz; Huseyin Baris Atakan; Irem Boybat; Alexandre Schmid; Yusuf Leblebici *EPFL, Switzerland; METU, Turkey; Sabanci University, Turkey*	**SIREN: A Depth-First Search Algorithm for the Filter Design Optimization Problem** Levent Aksoy; Paulo Flores; Jose Monteiro *INESC-ID, Portugal*
11:35	**A Source-synchronous Htree-based Network-on-Chip** Ayan Mandal; Sunil Khatri; Rabi Mahapatra *Texas A&M University, USA*	**Generating Concise Assertions with Complete Coverage** Chen-Hsuan Lin; Lingyi Liu; Shobha Vasudevan *University of Illinois at Urbana-Champaign, USA*
12:00	**A Parallel VLSI Architecture for Markov Chain Monte Carlo based MIMO Detection** Uwe Deidersen; Dominik Auras; Gerd Ascheid *RWTH Aachen University, Germany*	**Efficient Transistor-Level Design of CMOS Gates** Vinicius Possani; Vinicius Callegaro; Andre Reis; Renato Ribas; Felipe Marques; Leomar Rosa Junior *Universidade Federal de Pelotas, Brazil; Universidade Federal do Rio Grande do Sul, Brazil*
12:15	**Lunch - Room 351**	
13:30	**GLSVLSI Keynote - Room 351**	
	Clock Trees - Room 351 *Session Chair - Emre Salman, Stony Brook University, USA*	**Test 2 - Room 343** *Session Chair - Arne Heittmann - RWTH Aachen University, Germany*
14:30	**Assignment of Adjustable Delay Buffers for Clock Skew Minimization in Multi-Voltage Mode Designs** Jin-Tai Yan; Zhi-Wei Chen *Chung-Hua University, Taiwan*	**Combating NBTI-induced Aging in Data Caches** Shuai Wang; Guangshan Duan; Chuanlei Zheng; Tao Jin *Nanjing University, China*
14:45	**Variation-Aware Multi-Voltage Domain Clock Mesh Design** Can Sitik; Baris Taskin *Drexel University, USA*	**Performance/reliability trade-off in superscalar processors for aggressive NBTI restoration of functional units** Simone Corbetta; William Fornaciari *Politecnico di Milano, Italy*
15:00	**Coffee Break - Corridor, Level 3**	
	Reconfigurable - Room 351 *Session Chair - Sunil Khatri - Texas A&M, USA*	**VLSI Specialized Units - Room 343** *Session Chair - Ankur Srivastava - University of Maryland, USA*
15:15	**Delay Model for Reconfigurable Logic Gates Based on Graphene PN-junctions** Sandeep Miryala; Andrea Calimera; Enrico Macii; Massimo Poncino *Politecnico di Torino, Italy*	**On the Design of Modulo 2^n-1 Cubing Units** Evangelos Vassalos; Dimitris Bakalis *University of Patras, Greece*
15:40	**Analysis of the Area-Delay Performance of Hybrid Nanoelectronic Memory Cores Used in Field Programmable Gate Arrays** Arne Heittmann; Qin Wang; Tobias G. Noll *RWTH Aachen University, Germany*	**An Error Tolerant CAM with NAND Match-Line Organization** Aristides Efthymiou *University of Ioannina, Greece*
15:55	**DRMA: Dynamically Reconfigurable MPSoC Architecture** Lawrance Zhang; Jude Angelou Ambrose; Roshan Ragel; Swarnalatha Radhakrishnan; Jorgen Peddersen; Sri Parameswaran *University of New South Wales, Australia; University of Peradeniya, Sri Lanka; University of Wisconsin-Madison, USA*	**Efficient Modulo 2^n+1 Multiplication for the IDEA Block Cipher** Kiamal Pekmestzi; Constantinos Efstathiou; Nikos Moschopoulos; Kostas Tsoumanis *National Technical University of Athens, Greece; Technological Institute of Athens, Greece*
16:10	**A Compact FPGA-based Montgomery Multiplier over Prime Fields** Miguel Morales-Sandoval; Arturo Díaz-Pérez *CINVESTAV-LTI, Mexico*	**An Asymmetric Adaptive-Precision Energy-Efficient 3DIC Multiplier** Gopi Neela; Jeffrey Draper *University of Southern California, USA*
16:25	**Poster Session 2 - Corridor, Level 3**	
	CAD for 3D - Room 351 *Session Chair - Patrick Madden, SUNY Binghamton, USA*	**Design and Modeling - Room 343** *Session Chair - Guangyu Sun - Peking University, China*
16:55	**A Geometric Approach to Chip-Scale TSV Shield Placement for the Reduction of TSV Coupling in 3D-ICs** Caleb Serafy; Bing Shi; Ankur Srivastava *University of Maryland, USA*	**Multi-port FinFET SRAM Design** Yirong Zhao; Jiayin Li; Kartik Mohanram *University of Pittsburgh, USA*
17:20	**Thermal Stress Aware 3D-IC Statistical Static Timing Analysis** Bing Shi; Ankur Srivastava *University of Maryland, USA*	**Modeling Symmetrical Independent Gate FinFET using Predictive Technology Model** Mohammad Yousef Zarei; Reza Asadpour; Siamak Mohammadi; Ali Afzali-Kusha *Univerisity of Tehran, Iran*
17:55	**Effect of TSV Fabrication Technology on Power Distribution in 3D ICs** Suhas Satheesh; Emre Salman *NVIDIA, USA; Stony Brook University, USA*	**A Self-Tuning Multi-Objective Optimization Framework for Geometric Programming with Gate Sizing Applications** Amin Farshidi; Logan Rakai; Laleh Behjat; David Westwick *University of Calgary, Canada*
18:20	**Closing Session - Room 351**	
18:45	**Break**	
20:00	**Gala Dinner**	