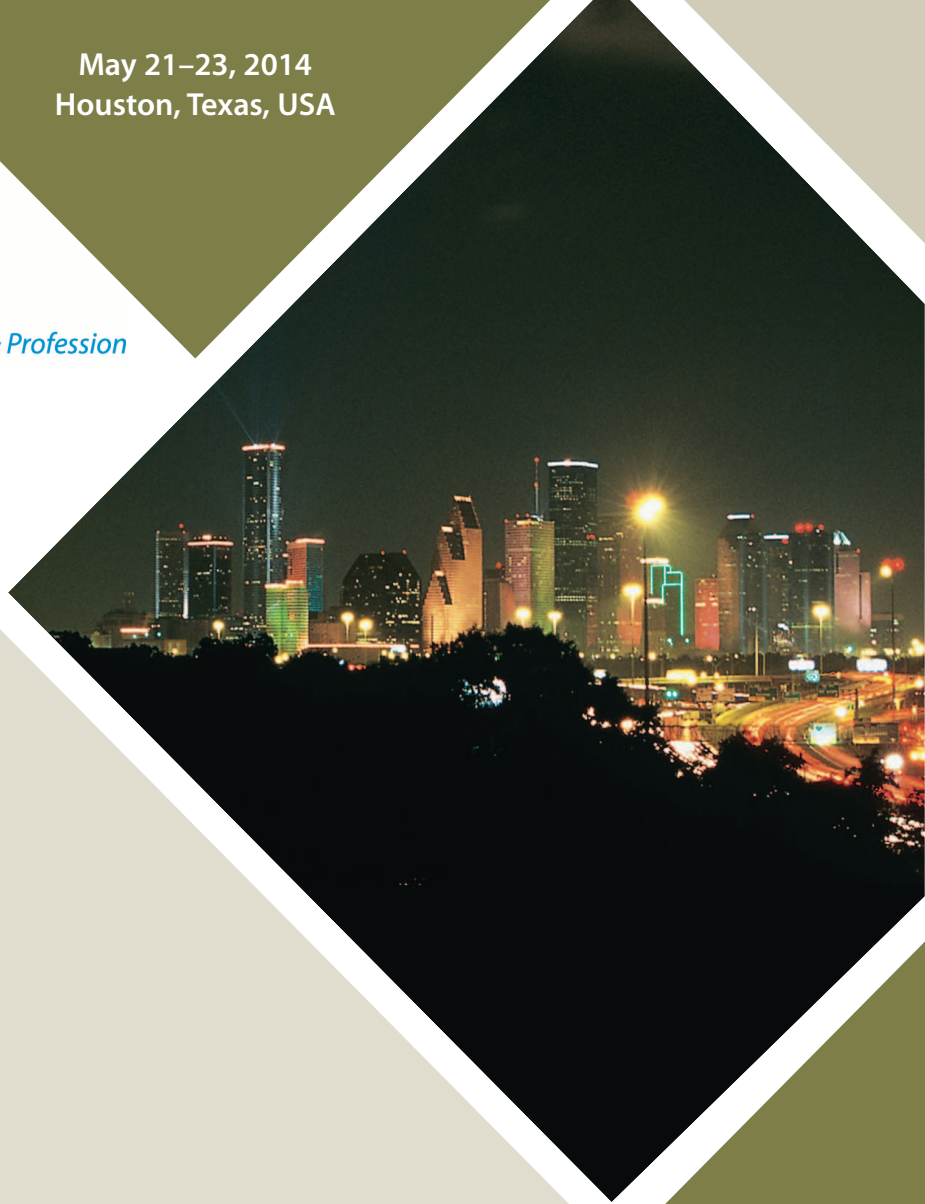


May 21–23, 2014  
Houston, Texas, USA



Association for  
Computing Machinery

*Advancing Computing as a Science & Profession*



# GLSVLSI'14

Proceedings of the 2014  
Great Lakes Symposium on VLSI

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## Tuesday, May 20, 2014

19:00 Welcome Reception

## Wednesday, May 21, 2014

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# WELCOME

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Welcome to the 24th edition of the Great Lakes Symposium on VLSI (GLSVLSI) 2014 held in Houston, Texas. GLSVLSI is a premier venue for the dissemination of manuscripts of the highest quality in all areas related to VLSI, devices and system level design. The venue of this year's GLSVLSI is Houston, which not only has a "Lake Houston" nearby but also is located right next to "Great Gulf of Mexico". You will enjoy the beautiful scenery surrounding Houston as well as the program over the two and a half days of this year's GLSVLSI activity.

As for the technical meeting, GLSVLSI 2014 was a resounding success: 179 papers were submitted, including authors from 30 different countries, of which 49 papers were accepted for oral presentation at the symposium (a 27.4% acceptance rate). With poster papers, a total of 76 papers will be presented at the symposium and published in the conference proceedings. The final technical program consists of 29 full presentations and 20 short presentations in 15 oral sessions and 27 posters in two poster sessions. Of these papers in the program, 55.8% are from North America, 18.2% from Asia, 20.8% from Europe, and 5.2% from South America/Australia.

GLSVLSI 2014 starts on Wednesday, May 21st, in the morning with an invited keynote talk "VLSI Systems for Neurocomputing and Health Informatics" by Keshab Parhi, University of Minnesota, followed by technical sessions on Reliability, CAD, Energy Efficient Systems, and System Design Methodologies, and an inspiring and entertaining dinner keynote talk "Create, then Innovate" by Gene Frantz. Then, the technical program continues on Thursday, May 22nd with the second invited keynote talk "Smart Nodes of Internet of Things (IoT): A Hardware Perspective View & Implementation" by Edgar Sanchez-Sinencio, Texas A&M University, followed by technical sessions which present the latest industrial and academic research covering topics such as Fault-tolerance, Application-specific Circuits and Systems, Reconfigurable Elements, and System-level Optimization. The conference will end by the noon of Friday, May 23rd after the third keynote talk "EDA for Extreme Scale Systems" by Alex Jones, University of Pittsburgh, and sessions on topics of Reconfigurable Systems, Analog Design, Low Power Design, and Emerging Technologies during the morning. Overall, there are 15 regular sessions in the technical program including a session where the "best paper award" candidates will have the opportunity to present their outstanding work.

Putting together GLSVLSI'14 was a team effort. We first thank the authors for providing the content of the program. We are grateful to the program committee, who worked very hard in reviewing papers and providing feedback for authors. Finally, we thank the hosting university, our sponsor, and ACM SIGs. We hope that you will find this program interesting and thought-provoking and that the symposium will provide you with a valuable opportunity to share ideas with other researchers and practitioners from institutions around the world.

**Joseph R. Cavallaro**  
GLSVLSI'14 General co-Chair  
Rice University, USA

**Tong Zhang**  
GLSVLSI'14 General co-Chair  
Rensselaer Polytechnic Inst., USA

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# TUESDAY, MAY 20, 2014

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19:00      **Welcome Reception, Garden Terrace Hilton Houston Plaza, 9th Floor**

# WEDNESDAY, MAY 21, 2014

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8:30      **Registration/Welcome, Pre-Function Space, BioScience Research Center (BRC)**

9:00      **Opening & Keynote I, Auditorium, BioScience Research Center (BRC)**

*Chair: Tong Zhang, Rensselaer Polytechnic Institute, USA*

*Speaker: Professor Keshab Parhi, University of Minnesota, USA*

*“VLSI Systems for Neurocomputing and Health Informatics”*

Abstract: Ubiquitous access to computers, cell phones, internet, personal digital devices, cameras and TV can be attributed to advances in the very large scale integration (VLSI) technology and the advances in circuit design to operate circuits at Gigahertz rates. One of the mysteries that we have not been able to unravel is the understanding of how the brain works from different perspectives. Reverse engineering the brain has been identified as one of the grand challenge problems by the National Academies. Advances in sensor technologies and imaging modalities such as electroencephalogram (EEG), intra-cranial electroencephalogram (iEEG), magnetoencephalogram (MEG), and magnetic resonance imaging (MRI) allow us to collect data from hundreds of electrodes from the brain at sample rates ranging from 256 Hz to 15kHz. These data can be key to not only understanding brain functioning and brain connectivity at macro and micro levels in healthy subjects but also in identifying patients with neurological and mental disorder. Extracting the appropriate biomarkers using spectral-temporal-spatial signal processing approaches and classifying states using machine learning approaches can assist clinicians in predicting and detecting seizures in epileptic patients, and in identifying patients with mental disorder such as schizophrenia, depression and personality disorder. The biomarkers can be tracked to design personalized therapy and effectiveness of therapy by closed loop drug delivery or closed loop neuromodulation, i.e., brain stimulation either by invasive or non-invasive means using electrical or magnetic stimulation. High-performance VLSI system design is critical to not-only increasing battery life of VLSI chips for neuromodulation but also for reducing computation time by orders of magnitude in analyzing MRI signals. Another grand challenge problem identified by the National Academies is Advanced Health Informatics. Analysis of health data is key to monitoring biomarkers and delivering drugs as needed. VLSI system design of biomarkers and disease state classification is again critical in improving the health and quality of life of human beings.

In this talk, I will highlight the emerging opportunities in high-performance low-power VLSI system design for neuro-computing and health informatics at various scales. At macroscale, the goal is to design small low-power implantable or wearable devices that can be used to monitor biomarkers and trigger an alarm signal to alert an abnormal state of the brain such as an impending seizure. At microscale, extracting thousands of connections from structural and functional MRI can require many hours or even a day for one subject and one set of parameters using parallel computers. The challenge here is to design parallel multicore computer architectures and compiler tools that can reduce the time for microscale analysis of MRI to an hour or less. I will describe research in my group in use of signal processing and machine learning approaches to identify and track various neurological and mental disorders. I will present some results on VLSI design of feature extractors such as power spectral density (PSD) and classifiers such as support vector machines (SVMs). I will present diabetic retinopathy screening using fundus image analysis and machine learning as an example to illustrate opportunities in design of embedded systems for health informatics. Significant research needs to be pursued in this area. My presentation will hopefully inspire further research in this emerging and important field of embedded VLSI system design for neuro, bio and health informatics.

10:30      **Coffee Break, Pre-Function Space**

# WEDNESDAY, MAY 21, 2014 (CONT'D)

## Session A, Auditorium

Reliability, Resiliency, Robustness 1  
Session Chair: Martin Margala  
University of Massachusetts, Lowell, USA

- 10:45** **Hardening QDI Circuits Against Transient Faults Using Delay-Insensitive Maxterm Synthesis**  
1Matheus Moreira, 1Ricardo Guazzelli, 1Guilherme Heck and 2Ney L. V. Calazans  
*1PUCRS, Brazil; 2FACIN-PUCRS, Brazil*
- 11:10** **System-Level Reliability Exploration Framework for Heterogeneous MPSoC**  
1Zheng Wang, 1Chao Chen, 2Piyush Sharma and 1Anupam Chattopadhyay  
*1RWTH-Aachen University, Germany; 2I.I.T. Patna, India*
- 11:35** **A TSV-Cross-Link-Based Approach to 3D-Clock Network Synthesis for Improved Robustness**  
Rickard Ewetz, Anirudh Udupa, Ganesh Subbarayan and Cheng-Kok Koh.  
*Purdue University*
- 11:55** **A Feasibility Study on Robust Programmable Delay Element Design Based on Neuron-MOS Mechanism**  
Renyuan Zhang and Mineo Kaneko  
*Japan Advanced Institute of Science and Technology, Japan*

## Session B, 2nd Floor Lecture Hall

CAD  
Session Chair: Yan Luo  
Oracle Inc. USA

- Horizontal Benchmark Extension for Improved Assessment of Physical CAD Research**  
Andrew B. Kahng, Hyein Lee and Jiajia Li  
*UCSD, USA*
- OCV-Aware Top-Level Clock Tree Optimization**  
1Tuck-Boon Chan, 1Kwangsoo Han, 1Andrew B. Kahng, 2Jae-Gon Lee and 1Siddhartha Nath  
*1UCSD, USA; 2Samsung Electronics Co., Ltd., USA*
- Modeling of the Charging Behavior of Li-Ion Batteries Based on Manufacturer's Data**  
Alessandro Sassone, Donghwa Shin, Alberto Bocca, Alberto Macii, Enrico Macii and Massimo Poncino  
*Politecnico di Torino, Italy*
- High Level Energy Modeling of Controller Logic in Data Caches**  
1Preeti Ranjan Panda, 2Sourav Roy, 2Srikanth Chandrasekaran, 1Namita Sharma, 1Jasleen Kaur, 1Sarath Kumar Kandam and 1Nagaraj N.  
*1Indian Institute of Technology Delhi, India; 2Freescale Semiconductor India Pvt. Ltd., India*

**12:15** **Lunch, 1st Floor Exhibit Hall**

## Best Paper Session, Auditorium

Session Chair: Alex K. Jones  
University of Pittsburgh, USA

- 13:30** **3D-SWIFT: A High-Performance 3D-Stacked Wide IO DRAM**  
1Tao Zhang, 1Cong Xu, 2Ke Chen, 3Guangyu Sun and 1Yuan Xie  
*1Pennsylvania State University, USA; 2Oracle Corp., USA; 3Peking University, China*
- 14:00** **Minimum Implant Area-Aware Gate Sizing and Placement**  
Andrew B. Kahng and Hyein Lee  
*UCSD, USA*
- 14:30** **A Multi-Stage Leakage Aware Resource Management Technique for Reconfigurable Architectures**  
Nam Khanh Pham, Amit Kumar Singh, and Akash Kumar  
*National University of Singapore, Singapore*

**15:00** **Coffee Break, 1st Floor Exhibit Hall**

# WEDNESDAY, MAY 21, 2014 (CONT'D)

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**15:15**      **Poster Session I, 1st Floor Exhibit Hall**  
Session Chair: Rung-Bin Lin  
Yuan Ze University, Taiwan

**A Performance Enhancing Hybrid Locally Mesh Globally Star NoC Topology**

1Tuhin Subhra Das, 1Prasun Ghosal, 2Saraju P. Mohanty and 2Elias Kougianos  
*1Bengal Engineering and Science University, Shibpu.*  
*2University of North Texas, USA.*

**VLSI Implementation of Linear MIMO Detection With Boosted Communications Performance**

Dominik Auras, Dominik Rieth, Rainer Leupers and Gerd Ascheid  
*RWTH Aachen University, Germany*

**Energy Optimal Sizing of FinFET Standard Cells Operating in Multiple Voltage Regimes Using Adaptive Independent Gate Control**

1Yue Fu, 2Yanzhi Wang, 2Xue Lin, 2Shahin Nazarian and 2Massoud Pedram  
*1 Oracle Corporation*  
*2University of Southern California, USA*

**A Low Power High Resolution Digital PWM with Process and Temperature Calibrations for Digital Controlled DC-DC Converters**

Jing Lu and Yong-Bin Kim  
*Northeastern University, USA*

**WeDBless: Weighted Deflection Bufferless Router for Mesh NoCs**

1Simi Zerine Sreeba, 2John Jose and 1Mini M.G.  
*1Model Engineering College, India. 2Rajagiri School of Engineering and Technology, Kochi, India*

**Trade-off between Energy and Quality of Service Through Dynamic Operand Truncation and Fusion**

Wenchao Qian, Robert Karam and Swarup Bhunia  
*Case Western Reserve University*

**A Novel Low-Power and In-place Split-Radix FFT Processor**

Zhuo Qian and Martin Margala  
*University of Massachusetts Lowell, USA*

**H.264 8x8 Inverse Transform Architecture Optimization**

Fabio Pereira, Andre Borin, Altamiro Susin, Aleksandro Bonatto and Marcelo Negreiros  
*UFRGS, Brazil*

**Energy-Efficient Wireless Network-on-Chip Architecture with Log-Periodic On-Chip Antennas**

1Md Shahriar Shamim, 1Naseef Mansoor, 2Aman Samaiyar, 1Amlan Ganguly, 3Sujay Deb and 3Shobha Sundar Ram  
*1Rochester Institute of Technology, USA. 2Delhi Technological University, India. 3Indraprastha Institute of Technology, India*

**Customizing an Open Source Processor to Fit in an Ultra-Low Power Cluster with a Shared L1 Memory**

1Michael Gautschi, 2Davide Rossi and 1,2Luca Benini  
*1ETH Zuerich, Switzerland. 2University of Bologna, Italy*

**Performance Modeling of Virtualized Custom Logic Computations**

Michael J. Hall and Roger D. Chamberlain  
*Washington University in St. Louis, USA*

**Scheduling of PDE Setting and Timing Tests for Post-Silicon Skew Tuning with Timing Margin**

Mineo Kaneko  
*Japan Advanced Institute of Science and Technology, Japan*

**An Area Efficient Low Power High Speed S-Box Implementation Using Power-Gated PLA**

Ho Joon Lee and Yong-Bin Kim  
*Northeastern University, USA*

**FPGA Based Implementation of a Genetic Algorithm for ARMA Model Parameters Identification**

Hocine Merabti and Daniel Massicotte  
*Université du Québec à Trois-Rivières, Canada*

**Highly Adaptive and Congestion-Aware Routing for 3D NoCs**

1Manoj Kumar, 1Vijay Laxmi, 1Manoj Gaur, 2Masoud Daneshtalab, 3Seok-Bum Ko and 4Mark Zwolinski  
*1Malaviya National Institute of Technology, Jaipur, India. 2University of Turku, Finland. 3University of Saskatchewan, Saskatoon, Canada. 4University of Southampton, UK*

# WEDNESDAY, MAY 21, 2014 (CONT'D)

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## Session A, Auditorium

Energy Efficient Systems

Session Chair: Alessandro Sassone

Politecnico di Torino, Italy

**16:15 Adaptive Compressive Sensing for Low Power Wireless Sensors**

Adam Watkins, Venkata Naresh Mudhiredy,  
Haibo Wang and Spyros Tragoudas  
*Southern Illinois University, USA*

**16:45 Regulator-Gating: Adaptive Management of On-Chip Voltage Regulators**

Selçuk Köse  
*University of South Florida, USA*

**17:15 Logic Block and Design Methodology for Via-Configurable Structured ASIC using Dual Supply Voltages**

1Ta-Kai Lin, 2Kuen-Wey Lin, 1Chang-Hao Chiu and  
1Rung-Bin Lin  
*1Yuan Ze University, Taiwan*  
*2 National Chiao Tung University*

**19:00 Gala Dinner, Hilton Room, Hilton Houston Plaza, 8th Floor**

Chair: Joseph Cavallaro, Rice University, USA

Speaker: Professor Gene Frantz, Rice University (formerly with Texas Instruments)

“Create, then Innovate”

## Session B, 2nd Floor Lecture Hall

Design Methodology

Session Chair: Ke Chen

Oracle Corporation

**Squash: A Scalable Quantum Mapper Considering Ancilla Sharing**

Mohammad Javad Dousti, Alireza Shafaei and Massoud Pedram  
*University of Southern California, USA*

**Design and Analysis of Robust and Wide Operating Low-Power Level-Shifter for Embedded Dynamic Random Access Memory**

Kenneth Ramclam and Swaroop Ghosh  
*University of South Florida, USA*

**A Study on the Use of Parallel Wiring Techniques for Sub-20nm Designs**

1Rickard Ewetz, 2Wen-Hao Liu, 3Kai-Yuan Chao, 2Ting-Chi Wang and 1Cheng-Kok Koh  
*1Purdue University, USA; 2National Tsing Hua University, Taiwan; 3Intel, USA*

Abstract: Innovation seems to be a measure of success for most technologists. We are proud of our innovations which have significantly contributed to society. But we seem not to speak much about creativity and how it relates to innovation. Is creativity part of the innovation process? Or is the innovation process the result of creativity? This talk will suggest an interesting set of definitions that put these two concepts into perspective. Examples will be shown that will support this proposed definitions.

# THURSDAY, MAY 22, 2014

**9:00 Keynote II, Auditorium, BioScience Research Center (BRC)**  
Chair: Joseph Cavallaro, Rice University, USA  
Speaker: Professor Edgar Sánchez-Sinencio, Texas A&M University  
“Smart Nodes of Internet of Things (IoT): A Hardware Perspective View & Implementation”

Abstract: A lot of efforts have been done on software layer to propose the idea of Internet of Things (IoT). However, the functionality of IoT highly depends on the implementation of its end nodes. And there is little attention about realization of such IoT Smart Nodes. As mixed signal IC researchers, we analyze the urgent needs of IoT Smart Nodes and their implementation challenges. We focus this talk on the two of the most important practical issues: energy harvesting & regulating, and wireless transceiver. A high efficient self-sustained energy harvester inside the Smart Nodes can power numerous possibilities to IoT network. For the various inputs, it should accommodate nonlinear energy sources and achieve Maximum Power Point Tracking (MPPT). As it is considered the most power hungry part, the wireless transceiver in the IoT Smart Nodes needs special focus to minimize its power consumption. The transceiver should adapt its power consumption based on the available amount of the energy and the amount of the transferred data in time.

## 10:00 Coffee Break, Pre-Function Space

**Session A, Auditorium, BRC**  
Reliability, Resiliency, Robustness II  
Session Chair - Dimin Niu  
Samsung Research, USA

**Session B, 2nd Floor Lecture Hall, BRC**  
Application Specific Designs  
Session Chair - Houman Homayoun  
George Mason University, USA

**10:15 WriteSmoothing: Improving Lifetime of Non-Volatile Caches Using Intra-set Wear-leveling**  
Sparsh Mittal, Jeffrey Vetter and Dong Li  
*1Oak Ridge National Laboratory, USA*

**A Hybrid Framework for Application Allocation and Scheduling in Multicore Systems with Energy Harvesting**  
Yi Xiang and Sudeep Pasricha  
*Colorado State University, USA*

**10:40 Reliability-Aware Cross-Point Resistive Memory Design**  
1Cong Xu, 1Dimin Niu, 1Yang Zheng, 2Shimeng Yu and 1Yuan Xie  
*1Pennsylvania State University, USA; 2Arizona State University, USA*

**Neural Network-Based Accelerators for Transcendental Function Approximation**  
Schuyler Eldridge, Florian Raudies, David Zou and Ajay Joshi  
*Boston University, USA*

**11:05 Using Adaptive Read Voltage Thresholds to Enhance the Reliability of MLC NAND Flash Memory Systems**  
1Nikolaos Papandreou, 1Thomas Parnell, 1Haralampos Pozidis, 1Thomas Mittelholzer, 1Evangelos Eleftheriou, 2Charles Camp, 2Thomas Griffin, 2Gary Tressler and 2Andrew Walls  
*1IBM Research - Zurich, Switzerland; 2IBM Systems and Technology Group, USA*

**Efficient Parallel Beamforming for 3D Ultrasound Imaging**  
1Pirmin Vogel, 1/2 Andrea Bartolini and 1/2 Luca Benini  
*1ETH Zurich, Switzerland*  
*2University of Bologna*

**11:25 A New Methodology for Reduced Cost of Resilience**  
Andrew B. Kahng, Seokhyeong Kang and Jiajia Li  
*UCSD, USA*

**A Task-Oriented Vision System**  
1Yang Xiao, 1Kevin Irick, 1Jack Sampson, 1Vijaykrishnan Narayanan and 2Chuanjun Zhang  
*1Pennsylvania State University, USA; 2Intel ISTC\_EC, USA*

## 11:45 Lunch, 1st Floor Exhibit Hall

# THURSDAY, MAY 22, 2014 (CONT'D)

## Session A, Auditorium

Memory Designs

Session Chair: Nikolaos Papandreou  
IBM Research GmbH, Zurich Research Laboratory

- 13:00 A New DRAM Architecture and its Control Method for the System Power Consumption**  
Yoshiro Riho and Kazuo Nakazato  
*Nagoya University, Japan*
- 13:25 A Memory Mapping Approach Based on Network Customization to Design Conflict-Free Parallel Hardware Architectures**  
Saeed Ur Rehman, Cyrille Chavet and Philippe Coussy  
*Université de Bretagne-Sud / Lab-STICC, France*
- 13:50 New 4T-Based DRAM Cell Designs**  
1Wei Wei, 2Kazuteru Namba and 1Fabrizio Lombardi  
*1Northeastern University, USA; 2Chiba University, Japan*

## Session B, 2nd Floor Lecture Hall

Fault Tolerance

Session Chair: Ann Gordon-Ross  
University of Florida, USA

- MB-FICA: Multi-bit Fault Injection and Coverage Analysis**  
Chen Jiang, Mojing Liu and Brett H. Meyer  
*McGill University, Canada*
- On-Line Detection of the Deadlocks Caused by Permanently Faulty Links in Quasi-Delay Insensitive Networks on Chip**  
Wei Song, Guangda Zhang and Jim Garside  
*University of Manchester, United Kingdom*
- A Novel Parallel Adaptation of an Implicit Path Delay Grading Method**  
Joseph Lenox and Spyros Tragoudas  
*SIU Carbondale, USA*

## 14:15 Coffee Break, 1st Floor Exhibit Hall

### 14:30 Poster Session II, 1st Floor Exhibit Hall

Session Chair: Prasun Ghosal  
Indian Institute of Engineering Science and Technology, Shibpur, India

#### Simscape Design Flow for Memristor Based Programmable Oscillators

Ebubechukwu Agu, Saraju Mohanty, Elias Kougianos and Mahesh Gautam  
*University of North Texas, USA*

#### Securely Outsourcing Power Grid Simulation on Cloud

Naval Gupte and Jia Wang  
*Illinois Institute of Technology, USA*

#### An Automated Design Approach to Map Applications on CGRAs

1Thomas Peyret, 1Gwenolé Corre, 1Mathieu Thevenin, 2Kevin Martin and 2Philippe Coussy  
*1CEA, LIST, France. 2Université de Bretagne-Sud, France*

#### He-P2012: Architectural Heterogeneity Exploration on a Scalable Many-Core Platform

1Francesco Conti, 2Chuck Pilkington, 3Andrea Marongiu and 1Luca Benini  
*1University of Bologna, Italy. 2STMicroelectronics, Canada*

#### On Macro-Fault: A New Fault Model, Its Implications On Fault Tolerance And Manufacturing Yield

1Tak-Kei Lam, 1King Wei, 2Wen-Ben Jone, 1Yi Diao and 1Yu-Liang Wu  
*1The Chinese University of Hong Kong, Hong Kong 2University of Cincinnati, USA*

#### Transient Analysis of Gate Inside Junctionless Transistor(GI-JLT)

Pankaj Kumar, P.N. Kondekar, and Sangeeta Singh  
*Indian Institute of Information Technology Design & Management, India*

#### Built-In Generation of Functional Broadside Tests Considering Primary Input Constraints

1Bo Yao, 1Irith Pomeranz, 2Srikanth Venkataraman and 2Enamul Amyeen  
*1Purdue University, USA. 2Intel Corporation, USA*

#### TSV Power Supply Array Electromigration Lifetime Analysis in 3D ICs

Qiaosha Zou, Tao Zhang, Cong Xu and Yuan Xie  
*Pennsylvania State University*

#### A Current-Mode CMOS/Memristor Hybrid Implementation of an Extreme Learning Machine

Cory Merkel and Dhireesha Kudithipudi  
*Rochester Institute of Technology, USA*

# THURSDAY, MAY 22, 2014 (CONT'D)

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14:30 **Poster Session II (Continued), 1st Floor Exhibit Hall**

**Modelling and Mitigation of Time-Zero Variability in sub-16nm FinFET-based STT-MRAM Memories**

Matthias Hartmann, Halil Kukner, Prashant Agrawal, Praveen Raghavan, Liesbet Van Der Perre and Wim Dehaene  
*IMEC VZW, KU Leuven, Belgium*

**A Design Flow for Physical Synthesis of Digital Cells with ASTRAN**

1Adriel Ziesemer Jr., 1Ricardo Reis, 2Matheus T. Moreira, 2Michel E. Arendt and 2Ney L. V. Calazans  
*1UFRGS, Brazil. 2PUCRS, Brazil*

**A Semi-Formal Approach for Analog Circuits Behavioral Properties Verification**

Ons Lahiouel, Henda Aridhi, Mohamed H. Zaki and Sofiene Tahar  
*Concordia University, Canada*

**Session A, Auditorium**

Reconfigurable Components

Session Chair: Karthikeyan Lingasubramanian  
University of Alabama at Birmingham, USA

**15:30 Reconfigurable STT-NV LUT-based Functional Units to Improve Performance in General-Purpose Processors**

1Adarsh Reddy Ashammagari, 2Hamid Mahmoodi, 3Tinoosh Mohsenin and 1Houman Homayoun  
*1George Mason University, USA; 2San Francisco State University, USA; 3University of Maryland Baltimore County, USA*

**15:55 A Generic Implementation of a Quantified Predictor on FPGAs**

Gervin Thomas, Ahmed Elhossini and Ben Juurlink  
*Technical University of Berlin, Germany*

**16:20 A Dual-Rail LUT for Reconfigurable Logic using Null Convention Logic**

Jing Yu and Paul Beckett  
*RMIT University, Australia*

**Session B, 2nd Floor Lecture Hall**

System Level Optimization

Session Chair: Selçuk Köse  
University of South Florida, USA

**A Complete Electronic Network Interface Architecture for Global Contention-Free Communication over Emerging Optical Networks-on-Chip**

1Marta Ortín-Obón, 2Luca Ramini, 2Herve Tatanguem Fankem, 1Victor Viñals and 2Davide Bertozzi  
*1University of Zaragoza, Spain; 2University of Ferrara, Italy*

**A Design Approach to Automatically Generate On-Chip Monitors during High-Level Synthesis of Hardware Accelerator**

1Mohamed Ben Hammouda, 2Philippe Coussy and 3Loic Lagadec  
*1Universite de Bretagne Occidentale, France; 2Universite de Bretagne-SUD, France; 3ENSTA-Bretagne, France*

**Thermal-aware Phase-based Tuning of Embedded Systems**

Tosiron Adegbiya and Ann Gordon-Ross  
*University of Florida, USA*

# FRIDAY, MAY 23, 2014

9:00

## Keynote III, 1st Floor Exhibit Hall

Chair: Hai (Helen) Li, University of Pittsburgh, USA

Speaker: Professor Alex Jones, University of Pittsburgh

“EDA for Extreme Scale Systems: Design Abstractions, Metrics, and Benchmarks”

Abstract: The context for EDA research is rapidly changing thanks to enhanced and novel switching devices, manufacturing technologies, new application targets, and the increasing software development effort required for new ICs. These trends continue to expand the gap between the capabilities of systems and what can be utilized by designers. To address these problems requires a collaborative effort with industry researchers, academics, and funding agencies working together in close partnership. This talk describes recommendations from the recent CCC workshop series on EDA in the Extreme Scale era for improving the collaboration between IC designers and EDA. There remains a continued importance of effective design abstractions that facilitate research on EDA advances that can be effectively translated to actual design flows for relevant technologies. Further, these abstractions must be accompanied by (i) effective design metrics, especially for new technologies where optimization objectives may not be obvious, and (ii) appropriate benchmarks, especially for more established technologies where alternative optimization techniques must be carefully compared. Focus on these research directions for EDA will have direct impact to reduce the existing capabilities gap between tools and designers.

10:00

## Coffee Break, Pre-Function Space

### Session A, Auditorium

Reconfigurable Systems

Session Chair: Xi Chen

Qualcomm Technology Inc. USA

### Session B, 2nd Floor Lecture Hall

Analog Design

Session Chair: Saraju Mohanty

University of North Texas, USA

**10:15 Hardware Trojan Attacks in FPGA Devices:  
Threat Analysis and Effective Countermeasures**

1Sanchita Mal-Sarkar, 2Aswin Krishna, 2Anandaroop Ghosh and 2Swarup Bhunia

1Cleveland State University, USA; 2Case Western Reserve University, USA

**Generation of Reduced Analog Circuit Models using Transient Simulation Traces**

1/2 Paul Winkler, 2Henda Aridhi, 2Mohamed H. Zaki and 2Sofiene Tahar

1Leipzigs University of Applied Sciences, Germany; 2Concordia University, Canada

**10:40 Forward-Scaling, Serially Equivalent Parallelism for FPGA Placement**

Christian Fobel, Gary Grewal and Deborah Stacey  
University of Guelph, Canada

**A Novel Mixed-Signal Self-Calibration Technique for Baseband Filters in Systems-on-Chip Mobile Transceivers**

Yongsuk Choi and Yong-Bin Kim  
Northeastern University, USA

**11:05 A Parallel and Reconfigurable Architecture for Efficient OMP Compressive Sensing Reconstruction**

1Amey Kulkarni, 2Houman Homayoun and 1Tinoosh Mohsenin

1University of Maryland, Baltimore County, USA; 2George Mason University, USA

**A Qualitative Simulation Approach for Verifying PLL Locking Property**

Ibtissem Seghaier, Henda Aridhi, Mohamed H. Zaki and Sofiene Tahar

Concordia University, Canada

11:25

## Break, Pre-Function Space

# FRIDAY, MAY 23, 2014 (CONT'D)

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## Session A, Auditorium

Low Power Design

Session Chair: Akash Kumar

National University of Singapore, Singapore

- 11:40** **Optimal Power Switch Design Methodology for Ultra Dynamic Voltage Scaling with a Limited Number of Power Rails**  
Yanzhi Wang, Xue Lin and Massoud Pedram  
*University of Southern California, USA*
- 12:00** **Level Shifter Planning for Timing Constrained Multi-Voltage SoC Floorplanning**  
Zhufei Chu, Yinshui Xia and Lunyao Wang  
*Ningbo University, China*
- 12:20** **Exploiting Heterogeneity in MPSoCs to Prevent Potential Trojan Propagation Across Malicious IPs**  
Chen Liu and Chengmo Yang  
*University of Delaware, USA*

**12:40** **Closing Session, Auditorium**

## Session B, 2nd Floor Lecture Hall

Emerging Technologies

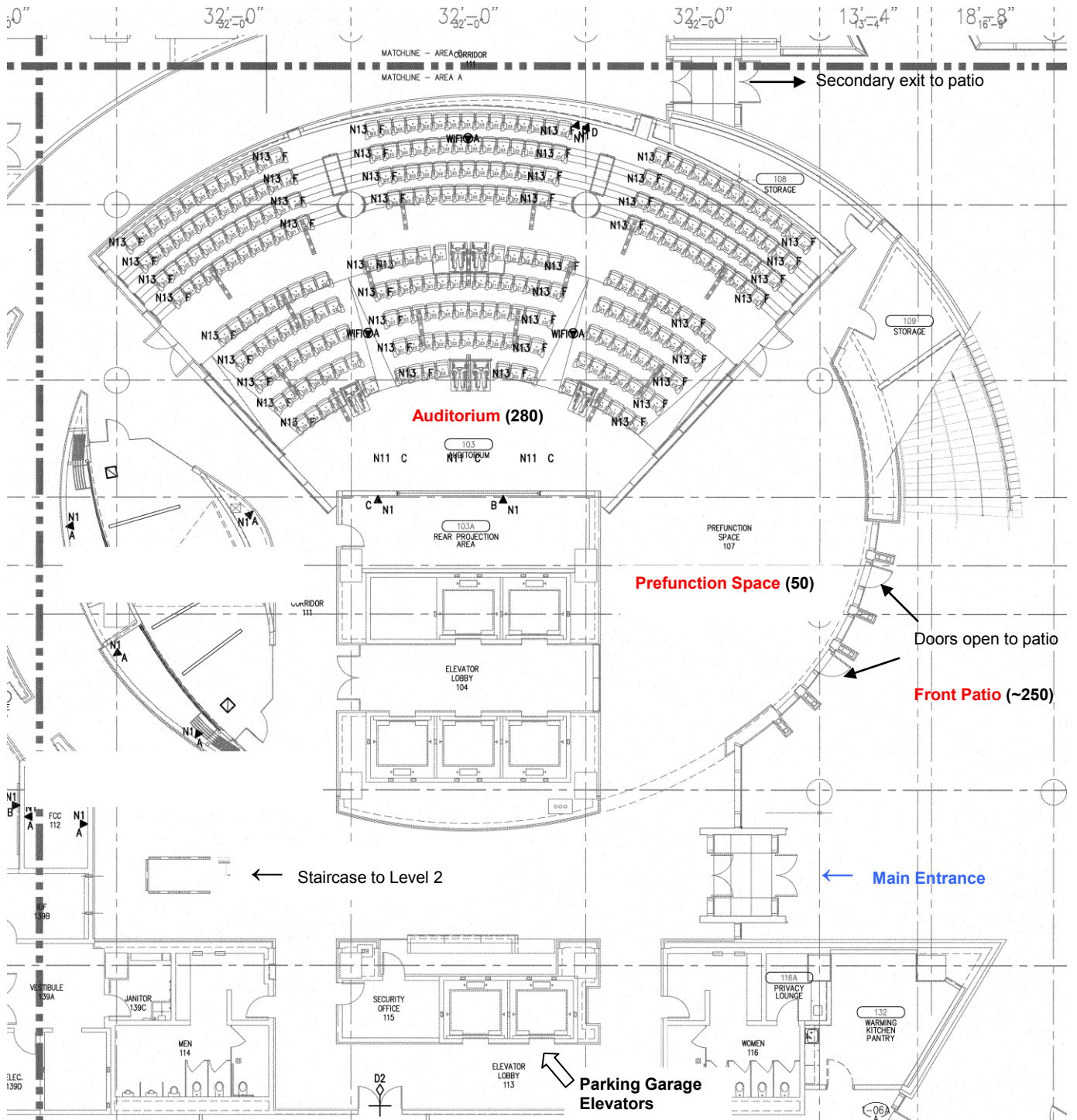
Session Chair: Zhenyu Sun

Broadcomm Inc., USA

- An Optically Reconfigurable Gate Array with an Angle-Multiplexed Holographic Memory**  
1Retsu Moriwaki, 2Hikaru Maekawa, 2Akifumi Ogiwara and 1Minoru Watanabe  
*1Shizuoka University, Japan; 2Kobe City College of Technology, Japan*
- Variability-Aware Design of Double Gate FinFET-based Current Mirrors**  
1Dhruva Ghai, 2Saraju Mohanty, 1Garima Thakral and 2Oghenekarho Okobiah  
*1Oriental University, India; 2University of North Texas, USA*
- A Comparison of FinFET Based FPGA LUT Designs**  
Monther Abusultan and Sunil Khatri  
*Texas A&M University, USA*

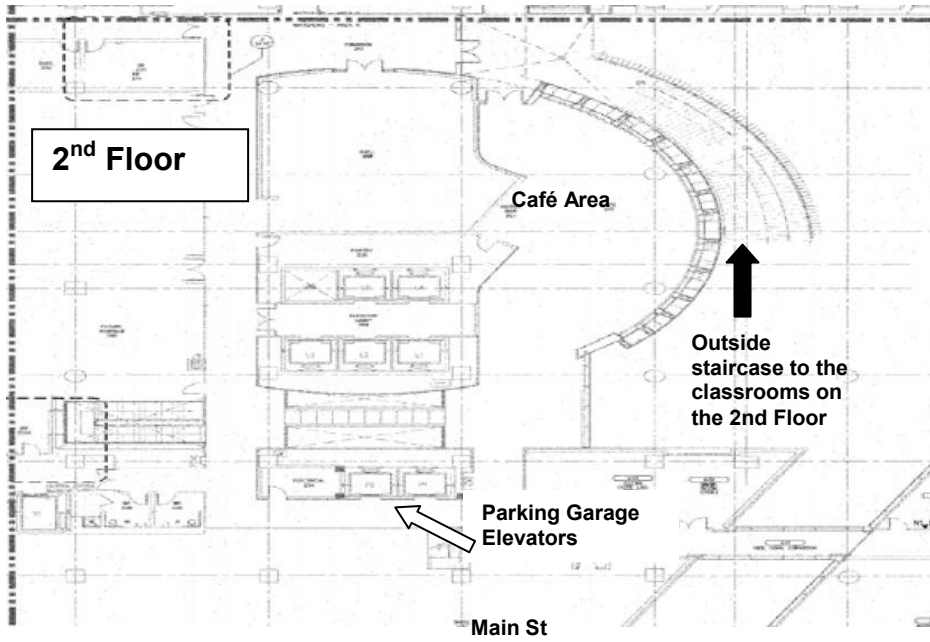
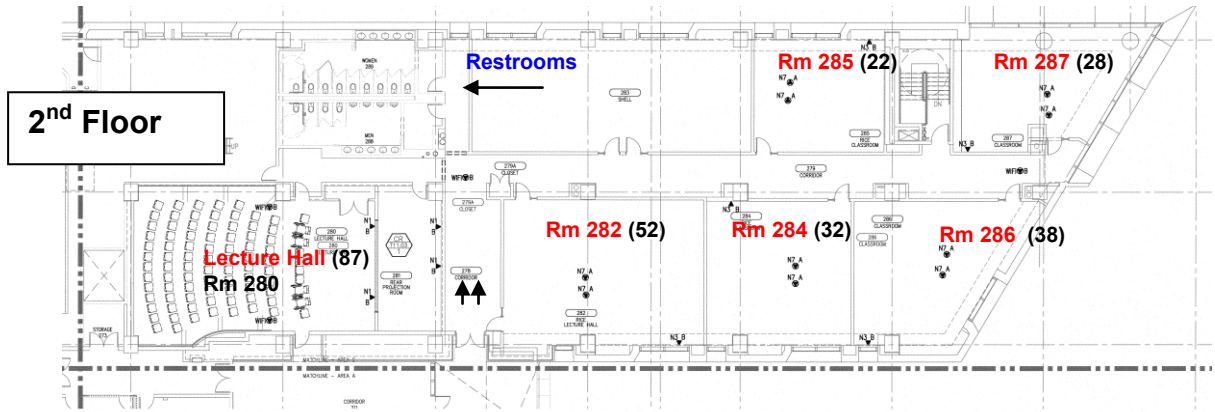
# MAPS

## BRC LEVEL 1



# MAPS (CONT'D)

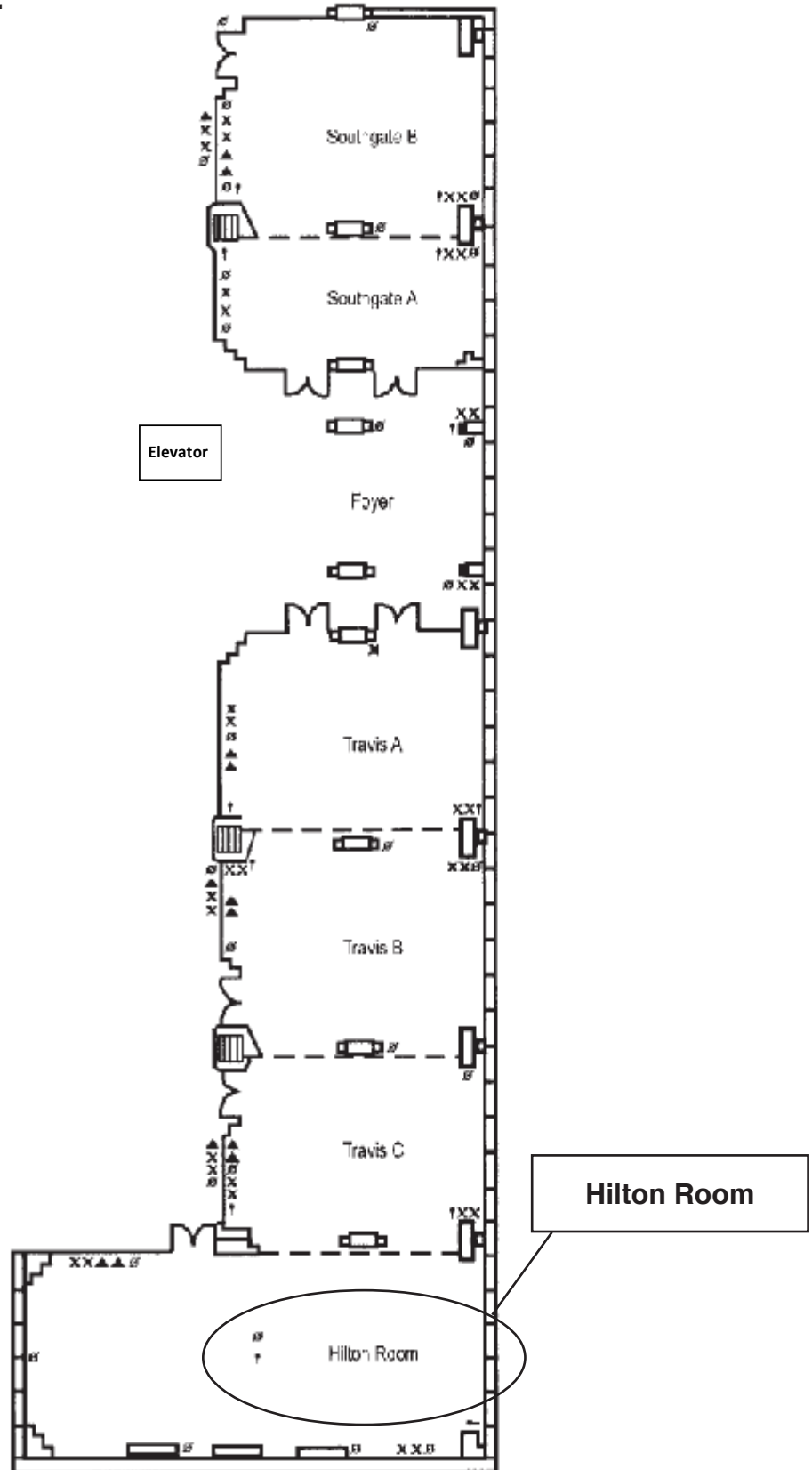
## BRC LEVEL 2



# MAPS (CONT'D)

Hilton Houston Plaza  
Garden Terrace is on 9th Floor

## 8th Floor:



# CALL FOR PAPERS



## GLSVLSI 2015

Pittsburgh, PA, USA, May 20-22 2015

<http://www.glsvlsi.org/>



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The 25th edition of GLSVLSI will be held in Pittsburgh, Pennsylvania, USA. Original, unpublished papers describing research in the general area of VLSI are solicited. Both theoretical and experimental research results are welcome. Proceedings will be published by the ACM and will be available through the ACM Digital Library. Please visit <http://www.glsvlsi.org/> for more information.

In addition to the traditional topic areas of GLSVLSI listed below, papers are solicited for a **special theme of healthcare and bioengineering, from circuits to systems**. We anticipate a special issue of a journal on the same topic for which selected papers related to the special theme will be invited to submit extended versions for consideration.

### Program Tracks:

- **VLSI Design:** design of ASICs, microprocessors/micro-architectures, embedded processors, analog/digital/mixed-signal systems, NoC, interconnects, memories, and FPGAs.
- **VLSI Circuits:** analog/digital/mixed-signal circuits, RF and communication circuits, chaos/neural/fuzzy-logic circuits, high-speed/low-power circuits.
- **Computer-Aided Design (CAD):** hardware/software co-design, logic and behavioral synthesis, logic mapping, simulation and formal verification, layout (partitioning, placement, routing, floorplanning, compaction), algorithms and complexity analysis.
- **Low Power and Power Aware Design:** circuits, micro-architectural techniques, thermal estimation and optimization, power estimation methodologies, and CAD tools.
- **Testing, Reliability, Fault-Tolerance:** digital/analog/mixed-signal testing, design for testability and reliability, online testing techniques, static and dynamic defect- and fault-recoverability, and variation-aware design.
- **Emerging Technologies & Post-CMOS VLSI:** nanotechnology, molecular electronics, quantum devices, biologically-inspired computing, spintronic technology, CNT, SET, RTD, QCA, VLSI aspects of sensor and sensor networks, etc. Emphasis should be on the analysis, novel circuits and architectures, modeling, CAD tools, and design methodologies for emerging technologies.

**Paper submission deadline:**

**December 9, 2014**

**Acceptance Notification:**

**February 3, 2015**

**Camera-Ready Paper Due:**

**February 24, 2015**

**Paper Submission:** Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered. Electronic submission in PDF format to the <http://www.glsvlsi.org> website is required. Author and contact information (name, affiliation, mailing address, telephone, fax, e-mail) must be entered during the submission process.

**Paper Format:** Submissions should be in camera-ready two-column format, following the ACM proceedings specifications located at:

<http://www.acm.org/sigs/pubs/proceed/template.html>

and the classification system detailed at: <http://www.acm.org/class/1998>

**Paper Publication and Presenter Registration:** Papers will be accepted for regular or poster presentation at the symposium. Every accepted paper MUST have at least one author registered to the symposium by the time the camera-ready paper is submitted; the author is also expected to attend the symposium and present the paper.



# SCHEDULE

|            | Time        | Auditorium                                        | 1st Floor Exhibit Hall | 2nd Floor Lecture Hall                  | Hilton                                                               | Pre-Function Space |
|------------|-------------|---------------------------------------------------|------------------------|-----------------------------------------|----------------------------------------------------------------------|--------------------|
| Tues. 5/20 | 19:00       |                                                   |                        |                                         | Welcome Reception, Garden Terrace<br>Hilton Houston Plaza, 9th Floor |                    |
|            | 8:30        |                                                   | Registration           |                                         |                                                                      |                    |
| Wed. 5/21  | 9:00        | Opening/Keynote I                                 |                        |                                         |                                                                      |                    |
|            | 10:30       |                                                   |                        |                                         |                                                                      | Coffee Break       |
|            | 10:45       | Session A: Reliability, Resiliency, Robustness I  |                        | Session B: CAD                          |                                                                      |                    |
|            | 12:15       |                                                   | Lunch                  |                                         |                                                                      |                    |
|            | 13:30       | Best Paper Session                                |                        |                                         |                                                                      |                    |
|            | 15:00       |                                                   | Coffee Break           |                                         |                                                                      |                    |
|            | 15:15       |                                                   | Poster Session I       |                                         |                                                                      |                    |
|            | 16:15       | Session A: Energy Efficient Systems               |                        | Session B: Design Methodology           |                                                                      |                    |
|            | 19:00       |                                                   |                        |                                         | Gala Dinner, Hilton Room, Hilton Houston Plaza, 8th Floor            |                    |
|            | Thurs. 5/22 | 9:00                                              | Keynote II             |                                         |                                                                      |                    |
| 10:00      |             |                                                   |                        |                                         |                                                                      | Coffee Break       |
| 10:15      |             | Session A: Reliability, Resiliency, Robustness II |                        | Session B: Application Specific Designs |                                                                      |                    |
| 11:45      |             |                                                   | Lunch                  |                                         |                                                                      |                    |
| 13:00      |             | Session A: Memory Designs                         |                        | Session B: Fault Tolerance              |                                                                      |                    |
| 14:15      |             |                                                   | Coffee Break           |                                         |                                                                      |                    |
| 14:30      |             |                                                   | Poster Session II      |                                         |                                                                      |                    |
| 15:30      |             | Session A: Reconfigurable Components              |                        | Session B: System Level Optimization    |                                                                      |                    |
| Fri. 5/23  | 9:00        |                                                   | Keynote III            |                                         |                                                                      |                    |
|            | 10:00       |                                                   |                        |                                         |                                                                      | Coffee Break       |
|            | 10:15       | Session A: Reconfigurable Systems                 |                        | Session B: Analog Design                |                                                                      |                    |
|            | 11:25       |                                                   |                        |                                         |                                                                      | Break              |
|            | 11:40       | Session A: Low Power Design                       |                        | Session B: Emerging Technologies        |                                                                      |                    |
|            | 12:40       | Closing Session                                   |                        |                                         |                                                                      |                    |