Paper Number	Title	Decision
1	Untrusted Third Party Digital IP cores: Power-Delay Trade-off Driven Exploration of Hardware Trojan Secured Datapath during High Level Synthesis	FULL PAPER - Long Presentation
2	Novel Designs of Embedded Hybrid Cells for High Performance Memory Circuits	POSTER
4	A Ternary Content Addressable Cell using a single Phase Change Memory (PCM)	FULL PAPER - Long Presentation
5	Design of Approximate Unsigned Integer Non-restoring Divider for Inexact Computing	FULL PAPER - Long Presentation
6	Dataline Isolated Differential Current Feed/Mode Sense Amplifier for Small Icell SRAM Using FinFET	POSTER
7	Efficient Test Application for Rapid Multi-Temperature Testing	FULL PAPER - Long Presentation
11	Multi Replica Bitline Delay Technique for Variation Tolerant Timing of SRAM Sense Amplifiers	FULL PAPER - Long Presentation
12	A Simulation Framework for Analyzing Transient Effects Due to Thermal Noise in Sub-Threshold Circuits	FULL PAPER - Short Presentation
13	Fine-Grained Voltage Boosting for Improving Yield in Near-Threshold Many-Core Processors	POSTER
16	A Reconfigurable Silicon-Photonic Network with Improved Channel Sharing for Multicore Architectures	FULL PAPER - Long Presentation
20	The Bit-Nibble-Byte MicroEngine (BnB) for Efficient Computing on Short Data	POSTER
26	Electromigration-aware Clock Tree Synthesis for TSV-based 3D-ICs	FULL PAPER - Long Presentation
27	DRAM based Intrinsic Physical Unclonable Functions for System Level Security	FULL PAPER - Short Presentation
32	Adaptive Bandwidth Management for Performance-Temperature Trade-offs in Heterogeneous HMC+DDRx Memory	FULL PAPER - Short Presentation
35	Space Oblivious Compression: Power Reduction for Non-Volatile Main Memories	POSTER
39	An Effective TSV Self-Repair Scheme for 3D-Stacked ICs	FULL PAPER - Short Presentation
43	Inevitability of Phase-locking in a Charge Pump Phase Lock Loop using Deductive Verification	FULL PAPER - Short Presentation
45	Reduced-latency LLR-based SC List Decoder for Polar Codes	POSTER
51	A Novel Framework for Temperature Dependence Aware Clock Skew Scheduling	FULL PAPER - Short Presentation
52	Approximate Multiplier Architectures Through Partial Product Perforation: Power-Area Tradeoffs Analysis	POSTER
53	Flip-Mirror-Rotate: An Architecture for Bit-write Reduction and Wear Leveling in Non-volatile Memories	POSTER
54	Characterizing the Activity Factor in NBTI Aging Models for Embedded Cores	POSTER
55	Characterization of SWCNT Bundle Based VLSI Interconnect with Self-heating Induced Scatterings	FULL PAPER - Short Presentation
57	Voltage-Boosted Synchronizers	FULL PAPER - Short Presentation
60	Yield-aware Performance-Cost Characterization for Multi-Core SIMT	POSTER
63	Improving Lifetime of Multicore Real-Time Systems through Global Utilization Control	POSTER
65	Phase-based Cache Locking for Embedded Systems	FULL PAPER - Long Presentation
67	Phase-based Instruction Window Optimization for Embedded Systems	POSTER
68	A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback	FULL PAPER - Long Presentation
69	Reinforcement learning for thermal-aware many-core task allocation	FULL PAPER - Short Presentation
70	Directed Self-Assembly Based Cut Mask Optimization for Unidirectional Design	POSTER
76	Efficient Reliability Analysis of Processor Datapath using Atomistic BTI Variability Models	FULL PAPER - Long Presentation
81	Analyzing the Tradeoff of Masking Multiple Errors with Configurable Bit-Width Voters	POSTER
83	Dynamic Bitstream Length Scaling Energy Effective Stochastic LDPC Decoding	POSTER
93	Speed Binning using Machine Learning and On-chip Slack Sensors	FULL PAPER - Short Presentation
94	Experimental Validation of a Faithful Binary Circuit Model	FULL PAPER - Long Presentation
100	Dynamically Reconfigurable RF NoC for Many-Core	FULL PAPER - Long Presentation
103	Sandwich Multilayer High Performance 3D Photonic Network-on-Chip	FULL PAPER - Long Presentation
105	Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line	FULL PAPER - Long Presentation
107	Small-World Network Enabled Energy Efficient and Robust 3D NoC Architectures	FULL PAPER - Long Presentation
110	Revisiting Dynamic Thermal Management Exploiting Inverse Thermal Dependence	FULL PAPER - Short Presentation
112	MSCS: Multi-hop Segmented Circuit Switching	FULL PAPER - Short Presentation

113	A Novel True Random Number Generator Design Leveraging Emerging Memristor Technology	FULL PAPER - Short Presentation
116	Runtime Power Reduction Techniques in On-Chip Photonic Interconnects	POSTER
118	TFET-based Operational Transconductance Amplifier Design for CNN Systems	FULL PAPER - Short Presentation
120	Playing with Fire: Transactional Memory Revisited for Error-Resilient and Energy-Efficient MPSoC Execution	FULL PAPER - Long Presentation
124	Reconfigurable - Self Adaptive Fault Tolerant Cache Memory for DVS enabled Systems	FULL PAPER - Short Presentation
127	Clock Skew Scheduling in the Presence of Heavily Gated Clock Networks	FULL PAPER - Long Presentation
131	Layout Characterization and Power Density Analysis for Shorted-Gate and Independent-Gate 7nm FinFET Standard Cells	FULL PAPER - Long Presentation
132	Skew Bounded Buffer Tree Resynthesis for Clock Power Optimization	POSTER
133	Lookup Table Based Discrete Gate Sizing for Delay Minimization with Modified Elmore Delay Model	FULL PAPER - Long Presentation
136	Delay, Power and Energy Tradeoffs in Deep Voltage-scaled FPGAs	POSTER
137	An Efficient Approach to Sample On-Chip Power Supplies	POSTER
140	Towards Statistial Verification of Analog and Mixed Signal Designs	POSTER
142	A Novel Static D Flip-Flop Topology for Low Swing Clocking	FULL PAPER - Short Presentation
145	Prediction of the Dark Silicon Phenomenon under Deeply-Scaled FinFET Devices	FULL PAPER - Short Presentation
154	Online and Operand-Aware Detection of Failures Utilizing False Alarm Vectors	FULL PAPER - Long Presentation
157	Exploiting the Expressive Power of Graphene Reconfigurable Gates via Post-Synthesis Optimization	FULL PAPER - Short Presentation
159	Design and Characterization of Analog-to-Digital Converters using Graphene PN-Junctions	FULL PAPER - Long Presentation
171	A Novel Technique for Optimizing VMIN of ROM Arrays	FULL PAPER - Short Presentation
175	Dynamic Task Priority Scaling for Thermal Management of Multi-core Processors with Heavy Workload	FULL PAPER - Short Presentation
179	BC-MIL-STD-1553+: Bus Controller for MIL-STD-1553B at 100-Mb/s Data Rate	FULL PAPER - Short Presentation